HIGH PERFORMANCE PHASE-LOCK LOOPS: APPLICATION TOWARDS INTEGRATED CMOS LOCK-IN AMPLIFIERS

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ABSTRACT

Phase-locked loop (PLL) and voltage-controlled oscillator (VCO) are widely used electronic components used in various applications such as frequency synthesis, data recovery, and skew compensation. PLL is also used in the development of lock-in amplifiers (LIAs). The LIA is extensively used in optical and physical measurement settings to extract weak signals embedded within high power ambient noise. The LIA relies on techniques such as noise filtering and phase-lock to extract the magnitude and phase of the input signal. PLL is used to generate the reference signal at the same frequency of the input signal with great signal spectral purity.

This dissertation focuses on the design and development of novel PLL, VCO and LIA circuitry. In particular, new techniques to improve the frequency tuning characteristics and phase noise of LC-VCO are studied and investigated. Also, high-speed integrated LIA in the MHz range based on fractional-N PLL is designed, where dynamic reserve as low as -30dB is achieved. The designed integrated LIA achieves satisfactory output dynamic range at a reasonable power consumption level, and has high integration potential compared to other existing table-top sized commercial LIAs.
RÉSUMÉ

Oscillateur à verrouillage de phase (PLL) et commandé en tension (VCO) sont largement utilisés des composants électroniques utilisés dans diverses applications telles que la synthèse de fréquence, les données de récupérer et de compensation de biais. PLL est également utilisé dans l'amplificateur à verrouillage (CER) de demande. La LIA est largement utilisé dans les paramètres optiques et physiques pour extraire un signal faible incorporé dans la puissance du bruit ambiant élevé. Le CER repose sur des techniques telles que le filtrage de bruit et à verrouillage de phase pour extraire l'amplitude et la phase du signal d'entrée. PLL est utilisée pour générer le signal de référence à la même fréquence du signal d'entrée avec la pureté spectrale du signal grande.

Cette thèse se concentre sur le développement du roman de PLL, VCO et LIA circuits. En particulier, les nouvelles techniques pour améliorer les caractéristiques de réglage de fréquence et de bruit de phase de LC-VCO sont étudiées et analysées. En outre, à haute vitesse intégrée LIA dans la gamme MHz basé sur N fractionnaire PLL est conçu, où réserve dynamique aussi bas que-30dB est atteint. Le conçu intégré LIA atteint la plage de sortie satisfaissante dynamique à un niveau de consommation électrique raisonnable, et a le potentiel d'intégration élevé par rapport à la LIA commerciale existante.
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CLAIMS OF ORIGINALITY

This dissertation focuses on the design and development of LC-VCO, PLL and LIA circuits. Four chip designs are presented, and the novelty of each design is summarized as follow:

1. The integrated LIA chip described in Chapter 2 targets the optical and spectroscopy application with very few off-chip components required. The design does not require external reference signal for the signal magnitude detection purpose, where the reference signal is generated using an internal PLL. This work was published in IEEE Transactions on Biomedical Circuits and Systems, vol. 4, no. 5, pp. 274-280, Oct. 2010.

2. An LC-VCO frequency tuning linearization technique is described in Chapter 3. The proposed technique improves the linearity of the tuning characteristic through the improvement of the varactor C(V) linearity. A new varactor configuration is proposed, and linearity of the frequency tuning characteristic is mathematically modeled. This work was published in Analog Integrated Circuits and Signal Processing, vol. 68, no. 3, pp. 307-314, Sept. 2011.

3. Chapter 4 describes a new time-weighted approach to model the LC-VCO oscillating frequency. The proposed model accounts for both the varactor
capacitance and switch transistor oxide capacitance over the oscillating cycle. Also, a new capacitor divider network and a notch filter are designed to improve the phase noise performance of the top-biased complementary LC-VCO. This work was published in Analog Integrated Circuits and Signal Processing, vol. 71, no. 2, pp. 197-210, May 2012.

4. Chapter 5 describes the design of a general-purpose high-speed fully integrated LIA. The LIA operates at 20MHz, and is able to extract the magnitude and phase of the input signal embedded within the ambient noise. The LIA relies on techniques such as noise filtering, time-averaging and phase-lock to recovery the input signal. This work was submitted to IEEE Transaction on Circuit and Systems I on June, 2012.

In particular, the high-speed LIA is the only integrated CMOS LIA to be ever developed for operation in the MHz input frequency range. The designed LIA provides satisfactory performance at a reasonable power consumption level. It provides an alternative solution for high-speed signal extraction with great freedom in system integration, and is much more economically feasible over the commercially available table-top size instruments.
CHAPTER 1: INTRODUCTION

1.1 Background

The history of phase-locked loop (PLL) is dated back to more than half a century ago, where the phase-lock technique is first used in wireless communication systems. The evolution of the PLL structure and design over time has adopted the PLL in widespread applications. Today, PLL can be found in almost every wired or wireless electronic communication system, and greatly affects the performance of the overall system. The functionality of the PLL is simple by a quick glance, where the PLL is able to generate an output signal with identical phase and frequency as the input signal. While these properties can be easily achieved with just a copper wire, the PLL offers several special properties making it unique:

1) Phase and frequency tracking: PLL is able to preserve the phase and frequency information of the input signal regardless of the variations of these two quantities.

2) Frequency multiplications: PLL is able to create output signal frequencies at any integer or fractional multiple times of the input signal frequency with great signal purity.

3) Phase noise filtering: Unlike many analog or digital filters targeted for frequency spectrum selection and rejection of the input signal, the PLL is able to alter the phase variation spectrum. This property is able to generate
output signal with extremely low noise, and operates as filters with very high quality factor.

Due to these special properties, PLLs have found wide applications in the following areas:

(1) Frequency synthesis: Frequency synthesizers in RF wireless transceivers use PLL to generate the desired reference frequency [1]-[3]. PLL with fast settling time generate a range of reference frequencies, where the mixers down-convert the input signal to the required baseband.

(2) Data recovery: Wire-line data communication relies on the clock-data recovery technique to transfer data between chips [4][5]. The clock is embedded within the data, and extracted with the PLL at the receiver end.

(3) Clock deskewing: Clock skew could potentially leads to malfunction of digital circuitry. PLL has been used to synchronize two separate clock paths and compensate for the time skew [6][7].

The voltage-controlled oscillator (VCO) is usually considered as the heart of the PLL structure. VCO is an autonomous circuit, which generates oscillating signals with variable frequency. The control signal of the VCO determines the oscillating signal frequency. Two main types of VCO exist namely the LC-VCO and the ring-VCO. The LC-VCO relies on the energy transfer between the capacitor and the inductor to generate the oscillating signal. The ring-VCO operates based on the principle of signal time delay and positive feedback. The
noise performance of the LC-VCO exceeds the ring VCO, and is mainly used in
the frequency synthesis application. On the other hand, the ring VCO has the
advantages of low power consumption and large frequency tuning range, and is
widely used in the data recovery and clock deskewing applications.

1.2 PLL Overview

The structure of a typical PLL is shown in Figure 1.1(a). An external crystal
oscillator with very precise frequency $F_{IN}$ drives a phase-frequency detector
(PFD). The PFD compares the phase and frequency difference between $F_{IN}$ and
the feedback signal $F_{FB}$. The charge pump generates a current signal, where the
polarity and the average magnitude of the current signal are proportional to the
phase difference between $F_{IN}$ and $F_{FB}$. The current signal is monitored by a loop
filter, which usually determines the overall loop dynamics such as the phase
margin and damping factor. The output signal of the loop filter $V_{TUNE}$ sets the
oscillating frequency $F_{OUT}$ of the VCO. The VCO frequency is usually much
higher than the crystal oscillator frequency. Therefore, $F_{OUT}$ is reduced by $N$ times
by a feedback divider, where,

$$F_{OUT} = NF_{FB}. \quad (1.1)$$

The loop dynamics are usually studied in the S-domain as modeled in Figure
1.1(b). The state variables are the phase variations of $F_{IN}$, $F_{OUT}$ and $F_{FB}$, and are
modeled by $\theta_1$, $\theta_2$ and $\theta'_2$, respectively. The PFD and the charge pump are
modeled together by a constant gain factor $K_{PFD}$. The loop filter is represented by
a transfer function, $F(s)$. The VCO gain $K_{VCO}$ measures the rate of frequency variation with respect to $V_{TUNE}$. As the VCO frequency changes, $\theta_2'$ accumulates over time as,

$$\theta_2' = \int \omega_{out} dt,$$  \hspace{1cm} (1.2)

and

Therefore, the VCO is modeled as $K_{VCO}/s$ in the S-domain. The feedback divider reduces $F_{OUT}$ by $N$ times. Even though the time difference between $F_{IN}$ and $F_{FB}$ is not changed by the feedback divider, the phase difference between $F_{IN}$ and $F_{FB}$ is reduced by $N$ times due to the frequency variation. When the PLL reaches the locked state, both the frequency and phase of $F_{IN}$ and $F_{FB}$ must be identical. The overall transfer function from the VCO output to the input is given by,
The transfer function from the feedback divider output to the input is given by,

\[
\frac{\theta_2}{\theta_1}(s) = \frac{NK_{pd}K_{VCO}F(s)}{Ns + K_{pd}K_{VCO}F(s)}. \tag{1.4}
\]

and the transfer function exhibits low-pass characteristics. As \(\theta_1\) changes slowly, \(\theta_2\) is able to track \(\theta_1\) closely, and the phase variation of \(\theta_1\) is inherited by \(\theta_2\) and \(\theta_2\)'.

When \(\theta_1\) changes rapidly, the PLL cannot respond fast enough to preserve the phase alignment between \(F_{IN}\) and \(F_{OUT}\). Therefore, the noise associated with the input signal at low frequency offset is passed to the output un-attenuated while the noise at high frequency offset is filtered.

### 1.2.1 Phase Frequency Detector and Charge Pump

The architecture of the typical PFD and the charge pump is shown in Figure 1.2:

![Figure 1.2: (a) PFD and current-mode charge pump. (b) PFD and charge pump operating characteristics.](image)
1.2(a). The PFD compares both the frequency and phase difference between the input and the feedback signal, and generates two output signals UP and DN. The relatively frequency and phase difference between \( \theta_{IN} \) and \( \theta_{FB} \) determine the polarity and pulse-width of UP and DN. The polarity of UP and DN determines if the charge pump current \( I_{CP} \) is sourced or sink from the loop filter, and the pulse-width of UP and DN determines the time-average magnitude of \( I_{CP} \). The variation of the time-average charge pump current \( I_{CP} \) with respect to the phase difference between \( \theta_{IN} \) and \( \theta_{FB} \) is shown in Figure 1.2(b), where a linear relationship exists under the ideal case. When \( \theta_{IN} \) aligns with \( \theta_{FB} \), the average charge pump current is zero. When \( \theta_{IN} \) leads or lags \( \theta_{FB} \) by \( 2\pi \), the charge pump sources or sinks \( I_{CP} \) from the loop filter. As a result, \( K_{PD} \) in Figure 1.1(b) is given by,

\[
K_{PD} = \frac{I_{CP}}{2\pi}.
\]

(1.6)

1.2.2 Loop Filter

The schematic of the current-mode passive loop filter is shown in Figure 1.3. The charge pump current \( I_{CP} \) is converted into \( V_{TUNE} \) through the loop filter, and

![Figure 1.3: Current-mode second-order passive loop filter.](image)
the transfer function $F(s)$ in Figure 1.1 is given by,

$$F(s) = \frac{V_{\text{TUNE}}}{I_{CP}} = \frac{sC_1R + 1}{s(sC_1C_2R + C_1 + C_2)}.$$  \hfill (1.7)

The transfer function exhibits two poles and one zero. The PLL loop dynamics can be conveniently set by adjusting the passive components values.

1.2.3 PLL Loop Dynamics

The open-loop transfer function of the PLL is given by,

$$G_{\text{loop}}(s) = K_{PD} F(s) = \frac{I_{CP} K_{VCO} (sC_1R + 1)}{2\pi s^2 (sC_1C_2R + C_1 + C_2)},$$  \hfill (1.8)

The transfer function consists of three poles with two poles at DC. Therefore, this type of PLL is also referred as Type-II. Due to the two poles at DC, the PLL is unstable, and a compensation zero is required for stability by adding the resistor

![Figure 1.4: Magnitude and phase response of the open-loop response.](image-url)
R. The bode plot of the open-loop response is shown in Figure 1.4. At \( \omega < \omega_Z \), the magnitude response decreases at -40dB/dec and the phase is at -180° due to the two poles at DC. At \( \omega_Z < \omega < \omega_P \), the magnitude response decreases at -20dB/dec. For \( \omega > \omega_P \), it becomes -40dB/dec again and the phase goes back to -180°. Within the vicinity of the crossover frequency \( \omega_C \), the loop filter transfer function \( F(s) \) can be approximated by \( R \) [8]. Here, \( \omega_C \) can be evaluated by setting the magnitude of (1.8) to 1 and replacing \( F(s) \) with \( R \). Therefore, the crossover frequency evaluates to,

\[
\omega_c = \frac{I_{cl}K_{vco}R}{2\pi}.
\]  

(1.9)

The relative location of the zero with respect to \( \omega_C \) has a huge impact on the loop stability where the damping factor is given by [9] as,

\[
\zeta = 0.5\sqrt{\frac{\omega_c}{\tau_z}}.
\]  

(1.10)

The further away the zero location is from \( \omega_C \), the loop stability gets better. However, the large zero time constant \( \tau_z \) requires large \( C_1 \) value which could be difficult to realize on-chip. Also, the pole location with respect to \( \omega_C \) also impacts the loop stability where the stability improves as the pole frequency increases. The pole frequency is mainly determined by \( C_2 \) where small \( C_2 \) value improves the stability. On the other hand, small \( C_2 \) value also leads to glitches of the PLL control voltage, which usually adds spurs to the PLL output signal spectrum.

The closed-loop response can be evaluated from (1.4) by substituting \( F(s) \) in (1.7) and is given by,
The error transfer function is given by,

\[
H_e(s) = \frac{1}{1 - H(s)} = \frac{\theta_e}{\theta_i} = \frac{s^3 + s^2 C_1 + C_2}{s^3 + s^2 C_1 + C_2 + s \frac{I_{CP}K_{VCO}}{C_1C_2R} + \frac{I_{CP}K_{VCO}}{2\pi NC_2} + \frac{I_{CP}K_{VCO}}{2\pi NC_1C_2R}}.
\]  
(1.12)

When a phase step is applied to the input signal, the phase error becomes,

\[
\theta_e(s) = \frac{\Delta \theta}{s} = \frac{s^3 + s^2 C_1 + C_2}{s^3 + s^2 C_1 + C_2 + s \frac{I_{CP}K_{VCO}}{C_1C_2R} + \frac{I_{CP}K_{VCO}}{2\pi NC_2} + \frac{I_{CP}K_{VCO}}{2\pi NC_1C_2R}} \Delta \theta.
\]  
(1.13)

As the time approach infinity, the phase error is evaluated with the final value theorem as,

\[
\theta_{e,\text{lim}}(\infty) = \lim_{s \to 0} s \theta_e(s) = 0.
\]  
(1.14)

Therefore, due to the disturbance of any phase displacement at the input, the phase error eventually becomes zero and the PLL reaches the locked state if enough time is given. Also, when a frequency step is applied to the input signal, the phase error becomes,

\[
\theta_e(s) = \frac{\Delta \theta}{s^2} = \frac{s^3 + s^2 C_1 + C_2}{s^3 + s^2 C_1 + C_2 + s \frac{I_{CP}K_{VCO}}{C_1C_2R} + \frac{I_{CP}K_{VCO}}{2\pi NC_2} + \frac{I_{CP}K_{VCO}}{2\pi NC_1C_2R}} \Delta \theta.
\]  
(1.15)

The phase error at the steady state is also evaluated by the final value theorem as,
This result shows that the PLL is able to recover from any frequency step and becomes locked again. Equations (1.14) and (1.16) show that the PLL is able to reach the locked state subject to input frequency and phase offset.

1.2.4 PLL Noise

The noise contributions due to individual PLL blocks are illustrated in Figure 1.5. The noise due to the PFD, loop filter, VCO and feedback divider are represented by $I_{\text{PD}}(s)$, $V_{\text{LF}}(s)$, $\theta_{\text{VCO}}(s)$, and $\theta_{\text{DIV}}(s)$. $\theta_{\text{VCO}}(s)$ and $\theta_{\text{DIV}}(s)$ are in rad$/\text{Hz}$ while $I_{\text{PD}}(s)$ and $V_{\text{LF}}(s)$ are in $\text{A}^2/\text{Hz}$ and $\text{V}^2/\text{Hz}$ [8]. The noise coming from the reference signal $\theta_1$, PFD, loop filter and feedback divider are shaped by the low-pass characteristics given by Equation (1.11). On the other hand, the noise due to the VCO is shaped by the high-pass transfer function given by Equation (1.12). Therefore, the overall noise at the PLL output is,

$$S_{\theta_2} = \left[H_1(s)\right]^2 + \left[H_2(s)\right]^2.$$  

Figure 1.5: Linear PLL noise model.
In general, the PLL output noise can be improved by decreasing the feedback divider $N$, decreasing $K_{VCO}$, decreasing $R_S$ in the loop filter, and increasing the charge pump current. Also, reducing the phase noise of the VCO and the feedback divider can also reduce PLL noise.

The PLL loop bandwidth also has an impact on the PLL noise performance. PLL with lower bandwidth greatly attenuates the noise coming from the reference signal but the majority of the VCO phase noise is passed to the VCO output. On the other hand, PLL with higher bandwidth attenuates VCO phase noise more effectively but the reference signal noise is unfiltered. Therefore, PLL loop bandwidth is designed mainly based on noise requirement for different applications. For frequency synthesis application, the PLL is driven by a crystal oscillator with extremely high frequency purity. Therefore, the PLL bandwidth is set much higher to suppress the VCO phase noise which usually dominates the PLL output noise. The upper bound on the PLL bandwidth is limited by PLL loop stability [10] where the loop bandwidth needs to be at least ten times less than the reference signal frequency for the developed continuous model to be valid.

1.2.5 PLL Architecture

The two major PLL architectures are the integer-$N$ PLL and fractional-$N$ PLL with advantages and disadvantages associated with each structure. The feedback divider of the integer-$N$ PLL in Figure 1.1 can only reduce the output frequency by integer-$N$ times as given by Equation (1.1). Therefore, the output frequency
resolution is limited by $F_{\text{IN}}$, where $F_{\text{OUT}}$ can only be changed by $F_{\text{IN}}$ increment. In order to improve the output frequency resolution, the reference frequency must decrease, which requires narrow PLL loop bandwidth for stability reason as described in the previous section. The drawbacks of narrow loop bandwidth include slow transient settling time and poor VCO phase noise rejection. Also, the feedback division ratio needs to increase, which degrades the PLL noise performance. Narrow PLL loop bandwidth and slow settling time are highly undesired traits for frequency synthesis applications.

To improve the PLL performance, the fractional-N PLL architecture is proposed where the feedback division ratio can be any fractional value. The most direct benefit of using a fractional feedback divider is that fine resolution at the PLL output can be achieved at much higher reference frequency and PLL loop bandwidth. The simplest way to achieve the fractional division is through the dual-counter divider shown in Figure 1.6 [8]. The VCO output signal $F_{\text{OUT}}$ is sent to a divider capable of dividing by $N$ or $N+1$. Two other counters control if the

![Figure 1.6: Dual-counter feedback divider.](image-url)
division value is $N$ or $N+1$. $F_{\text{OUT}}$ is divided by $N+1$ for $L$ cycles, and $N$ for $F-L$ cycles. Therefore, $F_{\text{OUT}}$ is related to $F_{\text{FB}}$ by,

$$F_{\text{OUT}} = F_{\text{FB}} \left( N + \frac{L}{F} \right).$$

(1.18)

Any arbitrary fractional division values can be achieved by setting $L$ and $F$, where the PLL output frequency resolution is $F_{\text{FB}}/F$. The drawback of this approach is that phase error exists for every $F_{\text{FB}}$ cycle with respect to the reference signal even in the locked state. The PLL never achieves the locked state as in the integer-$N$ PLL but the averaged PLL output frequency is given by Equation (1.18). The other drawback is that the $F_{\text{OUT}}$ is periodic with period $FT_{\text{FB}}$, which leads to fractional spurs at the PLL output signal spectrum located at $\pm mF_{\text{FB}}/F$. To filter out the reference spurs, an additional RC filter is usually added in the loop filter. The PLL output frequency resolution can be improved by increasing $F$. On the other hand, large $F$ value reduces the fractional spurs frequency, which can be difficult to filter out by the loop filter.

$\Delta \Sigma$ fractional-N feedback divider is proposed in Reference [11] to break the periodic pattern of the PLL output signal. The feedback division value is controlled by a $\Delta \Sigma$ modulator instead of digital counters. The noise transfer function of the $\Delta \Sigma$ modulator has high-pass characteristics, which effectively suppresses the quantization noise of the $\Delta \Sigma$ modulator and the cycle-to-cycle phase error. The high frequency quantization noise is suppressed by the low-pass characteristics of the PLL loop dynamics.
1.3 LC-VCO Overview

The LC-VCOs are widely employed in wireless transceivers and frequency synthesizers usually have the two structures as shown in Figure 1.7. The LC tank consists of the on-chip integrated inductor and the varactor with tunable capacitance implemented with $M_{6,7}$. The Switching transistor $M_{2,5}$ forms the negative resistance to compensate for the series resistance loss of the integrated inductor in order to sustain oscillation. Transistor $M_1$ provides constant current to the LC tank, where the oscillating amplitude is proportional to the drain current of $M_1$. The oscillating frequency is tunable by changing $V_{\text{Tune}}$, and the achievable frequency tuning range depends on a number of factors including the oscillating amplitude, varactor C-V characteristics and the parasitic capacitances associated with $M_{2,5}$.

Figure 1.7: (a) Top-biased PMOS LC-VCO. Top-biased complementary LC-VCO.
### 1.3.1 Integrated Inductor

The on-chip integrated inductor is generally implemented with the top metal layer available in the CMOS technology since:

1. The top-metal layer has relatively low sheet resistance due to the extra thickness of the metal layer.
2. The top metal layer has the largest distance from the substrate therefore the parasitic capacitances are much lower.

The inductance is designed with a spiral shape where the geometry of the inductor has a huge impact on the inductance value. The inductance consists of two components, the self-inductance of each metal strips and the mutual inductance between the metal strips. Some key geometry parameters of the inductor include the number of sides, the number of turns, the metal width, and the separation distance between adjacent turns.

The figure-of-merit of an inductor is the quality factor which is defined as,

\[
Q = \frac{\omega L}{R_s}
\]

where, \(\omega\), \(L\) and \(R_s\) are the signal frequency, inductance and series resistance of the inductor [12]. To improve the inductor quality factor, some general guidelines apply as:

1. The number of sides of the inductor is maximized to improve the mutual inductance between adjacent metal strips. As a result, the total inductance increases for the same series resistance.
2. The number of turns of the inductor needs to be set to an optimal value. The quality factor improves as the number of turns increases since both
the inductance and the resistance increase with respect to the number of
turns where the rate of the inductance increase is larger than that of the
resistance due to the multiplicity of the mutual inductance increase. The
upper bound of the number of turns is limited by the required inductance
value in order to achieve the desired oscillating frequency.

(3) The metal width also needs to be optimized. Wide metal width is usually
required to decrease the metal sheet resistance. On the other hand, wide
metal also increase the parasitic capacitance with respect to the substrate.
Moreover, the metal resistance increases with respect to the frequency due
to the skin effect where the electrons only travel beneath the metal surface
at high frequency [13]. Therefore, increasing metal width will no longer
improve the metal sheet resistance.

(4) The separation distance between adjacent metal turns is minimized to
increase the mutual inductance.
A guard ring is also placed under the inductor to reduce the magnetic field induced from the substrate current [14]. The lumped model described in [15] is widely used to characterize the on-chip inductor as shown in Figure 1.8. The inductance and the series resistance are modeled by L and Rs. The oxide capacitance between the top metal and the substrate are modeled as COX. The substrate resistance and capacitance are modeled by RSI and CSI. CO represents the coupling capacitance between the metal connections.

### 1.3.2 LC-VCO Start-up

The operating of the LC-VCO can be modeled by the RLC circuit as shown in Figure 1.9. The inductor and the varactor are modeled by passive inductor and capacitor. The inductor series resistor is converted into a parallel resistor through the approximation given by,

\[
R_s = \left(Q^2 + 1\right)R_p. \tag{1.20}
\]

The transconductance Gm represents the negative resistance formed by transistors M2-5. The parallel impedance formed by Rp, L and C is given by,

\[
Z_p = \frac{sR_p L}{s^2 R_p LC + sL + R_p}. \tag{1.21}
\]

At the resonant frequency, Zp evaluates to Rp and is purely resistive. The transfer function at the output is given by,

\[
(V_0 G_m) Z_p = V_0'. \tag{1.22}
\]
If the following conditions are satisfied then,

\[
\frac{V_o^{'}}{V_o} = G_m Z_p \geq 1, \quad \angle G_m Z_p = 180^\circ, \quad (1.23)
\]

oscillation at \( V_o \) will sustain. This condition is the well-known Barkhausen criterion used in system stability analysis. To ensure VCO start-up, \( G_m \) of LC-VCO is made at least two or three times larger than that of \( R_p \) by increasing transistor \( M_{2,5} \) aspect ratios.

Figure 1.9: Simplified LC-VCO model.

Figure 1.10: Simplified LC-VCO model.
1.3.3 LC-VCO Phase Noise

The LC-VCO phase noise is defined as the ratio of the noise power within 1Hz bandwidth at a frequency offset with respect to the carrier, and the carrier power. The noise associated with \( R_P \) is modeled by a current signal \( I_{n,Rp} \) as shown in Figure 1.10, which enters the LC tank with the transfer function,

\[
\frac{V_o}{I_{n,Rp}} = \frac{Z_p}{1-G_MZ_p}.
\]  
(1.24)

Therefore, the output noise power at a frequency offset \( \omega+\Delta\omega \) due to \( I_{n,Rp} \) is,

\[
\overline{V_o^2} = \left[ \frac{Z_p(\omega+\Delta\omega)}{1-G_MZ_p(\omega+\Delta\omega)} \right]^2 \left( I_{n,Rp} \right)^2.
\]  
(1.25)

\( I_{n,Rp} \) is modeled by the thermal noise of the resistor \( R_P \). The phase noise is derived by dividing the output noise power by the carrier power, and is given by,

\[
L(\omega_m) = \frac{4kTR_p}{A^2} \frac{1}{4Q^2} \left( \frac{\omega}{\omega_m} \right)^2 (1+F).
\]  
(1.26)

where, \( A \) is the oscillating signal amplitude, \( \omega_m \) is the frequency offset, \( \omega \) is the

Figure 1.11: Typical LC-VCO phase noise model.
carrier frequency, Q is the inductor quality factor, and F is the noise factor of the active devices. The phase noise model in Equation (1.26) is the Leeson’s phase noise model [16], where a typical LC-VCO phase noise spectrum is shown in Figure 1.11. At low frequency offset, the phase noise spectrum decreases at -30dB/dec where the upconverted flicker noise of the biasing transistor dominates. As the frequency offset increases, the phase noise spectrum decreases at -20dB/dec, and the upconverted thermal noise of $R_P$ and biasing transistor dominates. At high frequency offset, the VCO phase noise is dominated by the thermal noise of $R_P$. The noise factor in (1.26) is expressed as,

$$
F = 1 + \frac{4\gamma IR}{\pi A_o} + \frac{4}{9} g_{m,\text{bias}} R_P,
$$

where, the three terms represent the noise contributions from $R_P$, the switching transistor, and the biasing transistors [17].

To improve the phase noise performance of LC-VCO, some general guidelines apply:

1. High inductor quality factor can greatly improve the phase noise performance where the phase noise can be improved up to 6dB by doubling the inductor quality factor.

2. Large signal amplitude also improves the phase noise performance at the cost of power consumption.

3. Reducing the noise factor F is also effective, which requires optimization of the aspect ratios of the biasing and switching transistors.
The oscillating signal amplitude variation with respect to the biasing current is shown in Figure 1.12. When the biasing current is less than $I_{OPT}$, the signal amplitude increases linearly with respect to the bias current, where the VCO operates in the current-limited region. The signal amplitude is eventually bounded by the operating point of the switching transistors, and further increase of the biasing current no longer increases the signal amplitude. The VCO operates in the voltage-limited mode, where the signal amplitude stays constant with respect to the biasing current. Therefore, for optimal phase noise without excessive power consumption, $I_{BIAS}$ should be set within the vicinity of $I_{OPT}$. The figure-of-merit (FoM) of the LC-VCO is given by,

$$FoM = \frac{1}{L \cdot P} \left( \frac{\omega}{\omega_m} \right)^2,$$

which accounts for the VCO phase noise, power consumption and frequency offset. The FoM is convenient for comparing VCO performances operating at different carrier frequencies.

Figure 1.12: Oscillating signal variation with respect to the biasing current.
1.3.4 LC-VCO Topology

The two common LC-VCO topologies shown in Figure 1.7 are widely used in wireless and communication systems. For the same biasing current, the oscillating signal amplitude of the complementary VCO is almost twice compared to the signal amplitude of the PMOS VCO. Therefore, the complementary VCO is the preferred choice for low power applications. As the biasing current increases, the signal amplitude of the complementary VCO is limited by the switching transistors. On the other hand, the signal amplitude of the PMOS VCO can grow to a much larger value. Therefore, the PMOS VCO is the preferred choice if good phase noise performance is the primary consideration.

1.4 PLL in Lock-In Amplifier

Other than the aforementioned three major applications of the PLL, there are a number of other applications where PLL is employed, and one of these applications is the lock-in amplifier (LIA). The LIAs are widely used systems in physical and chemical sensing and materials spectroscopy applications [18]-[25]. LIAs aim to solve a common problem encountered in the data acquisition of weak (small amplitude current or voltage) signals that are distorted by noisy background signals. In short, LIAs improve the signal to noise ratio of the signal and are the preferred choice in applications where the desired output signal is usually embedded within considerable noise power and in many situations with noise power many times more than that of the desired signal [3-5].
The function of the PLL in the LIA is similar to that in the wireless transceivers. The PLL generates the reference signal with the same frequency as the input signal. The mixer down-converts the input signal to DC based on the reference signal. Since the input signal is within the kHz range, LC-VCO is not feasible to integrate and ring-VCO is usually implemented.

1.5 Thesis Contributions and Organizations

The contributions of this dissertation are to improve LC-VCO and PLL performance from the circuit perspective, and improve the overall performance of the LIA in return. Four projects are undertaken and presented in the following order:

Chapter 2 presents the design details of a CMOS optoelectronic LIA for sensing and spectroscopy application. The design uses a phototransistor array to convert the incident optical signals into electrical currents. The photocurrents are then converted into voltage signals using a transimpedance amplifier for subsequent convenient signal processing by the LIA circuitry. The noise and signal distortions are suppressed with filters and PLL implemented in the LIA, and the output DC voltage is directly proportionally to the input optical power.

In Chapter 3, an oscillation frequency linearization technique for LC-VCO with an inversion-mode varactor is proposed. The linearity of the frequency tuning curve is improved by linearization of C(V) characteristics of the inversion-
mode varactor. A new varactor configuration consisting of varactor units and resistor divider network is proposed. The single-switch integrated LC-VCO with the proposed varactor configuration is fabricated in TSMC 0.18\(\mu\)m CMOS technology. The improvement of linearity of the frequency tuning curve has been verified using mathematical models and measurement results.

Chapter 4 presents the design and development of a low-power LC-VCO with improved phase noise performance by implementing a new capacitor divider varactor configuration and a 2\(^{nd}\) order notch filter. Also, this chapter presents a new time-weighted approach to model the effective capacitance experienced by the oscillating signal over the oscillation period.

In chapter 5, a general-purpose high-speed integrated LIA is designed, which consists of the magnitude and phase measurement circuitry components to extract the input signal magnitude and phase where the SNR can be as worse as -30dB. The magnitude measurement circuitry relies on the band-pass filter and a current integrator to generate the \(V_{\text{MAG}}\) signal where \(V_{\text{MAG}}\) is directly proportional to the input signal amplitude. The phase measurement circuitry uses a low-bandwidth PLL and current integrator to generate the \(V_{\text{PH}}\) where \(V_{\text{PH}}\) is directly proportional to the phase difference between the input signal and the reference signal. The designed LIA is fully integrated and requires no off-chip components.

The dissertation is concluded in Chapter 6.
CHAPTER 2: CMOS OPTOELECTRONIC LIA

In this chapter, a CMOS optoelectronic LIA for sensing and spectroscopy application is presented. In the lock-in-amplification technique, the signal obtained from the input/sensing interface is modulated at a known frequency. The signal is multiplied with a known reference signal of the same frequency as the input signal. The multiplied product signal is then down-converted to a low-frequency signal from which the amplitude and phase of the desired signal is extracted. To date, there have been many implementations of LIA in CMOS technology. For example, in Johnson et al. [18], the LIA is used to monitor exocytosis variation by measuring the changes in cell membrane capacitance. The input signal was modulated by a pair of quadrature reference signals. The LIA generated the full-wave rectification of the input signal where the DC component is filtered out. The system operates at 1.5kHz. The input signal amplitude is at 50mV, and the output signal range is from 0.1V to 1V. In De Marcellis et al. [20], a low-frequency LIA operating under 100Hz frequency is proposed. The input signal is first processed by a low-noise amplifier (LNA) and a band-pass filter. Then, the signal is down-converted to the baseband by a mixer where the DC component was filtered out by a low-pass filter. The design was implemented in CMOS 0.35µm technology where the intrinsic gain of the LIA was measured to be 5691V/V. In Gnudi et al. [21], the structure of the proposed LIA is similar to the structure described in [20]. The design was fabricated in CMOS 0.7µm technology, and consumed 25mW static power. The system operated at 20kHz,
and was capable of extracting signals as small as 100nV from the ambient noise. In Azzolini et al. [22], the LIA was used to detect low-level signals in magnetically excited resonant structures. The input signal was modulated by a pair of quadrature signals where the reference signal was generated by a PLL. The design was fabricated in CMOS 0.35µm technology, and consumed 110mW static power. That system was capable of extracting signals of 1µV at 30kHz.

In this Chapter, we describe the design and development of a low-power monolithically integrated optoelectronic LIA implemented in TSMC 0.35µm CMOS technology. Optoelectronic LIAs are indispensable in optical materials spectroscopy and can be very useful in optical (luminescence)-based biological and chemical sensing. The developed LIA includes a high gain photo-transistor array to convert the incident optical signals into electrical current signals. The photocurrent is then amplified and converted into a voltage signal by a transimpedance amplifier which is then processed by the LIA circuitry. Here, we focus on luminescence intensity monitoring applications where we aim to extract only the amplitude of the input signal. Thus, for the aforementioned specific application, we propose a new architecture that does not require an external reference signal since the reference signal is generated internally using a PLL. We examined the functionality of the LIA using a LED as the optical source. This is done since most low-power optical sensors prefer the use of an LED as the excitation source. The proposed LIA consumes an average power of 12.79mW with 3.3V power supply, and its operating frequency range is from 13kHz to
25kHz. This frequency bandwidth is selected since it is the optimum range in many sensing and spectroscopy applications [26]-[28].

### 2.1 Optoelectronic Lock-in Amplifier

The block diagram of the designed optoelectronic lock-in amplifier is shown in Figure 2.1. The input optical signals are sinusoidal modulated before they impinge on the LIA. The on-chip phototransistor array detects the incident optical signals and generates a proportional electrical current. The photo-current signal can be expressed as,

\[
I(t) = I_o \cos(\omega_o t) + I_D,
\]

where, \(I_o\) is the peak current intensity, \(I_D\) is the photo transistor dark current, and \(\omega_o\) is the LED modulating angular frequency. The current signal is converted into a voltage signal through a high-gain transimpedance amplifier where the DC and AC components of the current are amplified. The high-pass filter after the TIA removes the undesired DC offset voltage. The output signal is then processed by a band-pass filter to remove the noise and the interference with tones other than \(\omega_o\). The high-pass filter after the band-pass filter then removes the DC offset voltage introduced by the band-pass filter. Next, the signal is amplified to rail-to-rail amplitude by an amplifier, and the amplifier output signal drives a PLL. The PLL

![Figure 2.1: System diagram of the designed lock-in amplifier](image)
provides a single tone at $\omega_o$ with very small side-bands associated with $\omega_o$. As a result, the PLL output spectrum resembles that of a band-pass filter with a very high quality factor. The PLL output and the output signal after the second high-pass filter are sent to a mixer. Since the PLL output side-band magnitudes are very small, the noise power down-converted to the base-band is greatly reduced. The mixer output signal can be expressed as,

$$V(t) = I_o A + I_o A \cos(2\omega_o t),$$  

(2.2)

where, $A$ is the accumulated gain of the TIA, high-pass filter, band-pass filter, and the mixer. $V(t)$ consists of two tones located at the DC and $2\omega_o$, respectively. A low-pass filter is added after the mixer to remove the tone at $2\omega_o$. Therefore, the low-pass filter output signal, $V_{out}$ (which is a dc voltage) is directly proportional to the photo-current $I_o$, where $I_o$ is proportional to the incident optical power. The rest of this section describes the operation of each functional block in details.

### 2.1.1 Photo-transistor Array

The incident light is detected by an $11 \times 18$ phototransistor array. The microphotograph of an array of six phototransistor pixels is shown in Figure 2.2. The area of each photo-transistor is $35\mu m \times 35\mu m$, and the overall area of the photo-transistor array is $400\mu m \times 640\mu m$. The structure of the photo-transistor pixel is similar to a bipolar junction transistor formed by P-active(emitter) / N-well(base) / P-substrate(collector). The phototransistor is designed so that all of the emitter terminals are connected to the input of the TIA, and the collector terminals are connected to the ground. This vertical phototransistor structure has
demonstrated good responsively in the visible region of the electromagnetic spectrum [26]-[28]. The bandwidth of the photo transistors is few hundred kilo-hertz which covers the intended operating frequency range of the proposed LIA. The vertical phototransistor architecture can produce currents that are several times larger than a comparable sized photodiode which is required for detecting low amplitude luminescence signals in sensing and spectroscopy [27][28].

2.1.2 Transimpedance Amplifier (TIA)

The TIA serves the purpose of converting the generated photo-current signal $I_{in}$ into a voltage signal $V_{out}$. The circuit schematic is shown in Figure 2.3. The bias voltages are provided off-chip. $M_3$ and $M_4$ are stacked to increase the TIA transimpedance. The output DC voltage is forced to be approximately equal to $V_{bx}$ through replica biasing circuitry. The amplifier used in the replica biasing circuitry is a standard 5-transistors differential to single-ended configuration. The simulated performance of the TIA demonstrated large trans-impedance (120dBΩ), good linearity, and relatively low noise (7.878pA/√Hz). The transimpedance is approximated by,

Figure 2.2: Microphotograph of a single photo-transistor pixel.
Figure 2.3: Circuit schematic of the TIA. Transistor sizes: $W_1 = 50\mu m$, $W_2 = 40\mu m$, $W_{3,4} = 200\mu m$, $L_{1-4} = 8\mu m$. $V_{b1} = V_{b2} = V_{bx} = 1.6V$, $V_{b3} = 1.2V$.

\[
\frac{V_{out}(s)}{I_{in}} = \frac{g_{m2}r_{o2}}{sC_{gs2} + g_{m2}},
\]

(2.3)

where, the low-frequency trans-impedance is $r_{o2}$, and the bandwidth is $\frac{g_{m2}}{C_{gs2}}$. $r_{o2}$ can be enlarged by increasing the aspect ratio of $M_2$ at the cost of linearity, noise performance and power consumption. The simulated TIA bandwidth is 303.5kHz, which exceeds the targeted operating range of 13kHz to 25kHz.

2.1.3 High-Pass Filter

The photo-transistor output currents include a DC and an AC component where both components are amplified by the TIA. While the AC component does not affect the output DC voltage, the DC component leads to an undesired DC offset voltage at the output which imposes an unintended biasing voltage on the downstream signal processing stages. Therefore, a high-pass filter is added after the TIA to remove the undesired DC offset voltage. The schematic of the designed high-pass filter is shown in Figure 2.4(a). This topology is taken from
[29] and consists of two operational-transconductance amplifiers (OTAs) and two capacitors $C_1$ and $C_2$. The capacitors are implemented on chip. The schematic of the OTAs is shown in Figure 2.4(b). The positive, negative and output terminals of $G_{m2}$ form the unity-gain feedback configuration such that $V_{out}$ follows $V_{c1}$. $G_{m1}$ and $C_1$ are added on top of this configuration to increase the order of the filter by one. Since, $V_{out}$ follows $V_{c1}$, $V_{out}$ also follows $V_{b1}$. Therefore, the output DC voltage of the high-pass filter is set by $V_{b1}$. The input to output transfer function is,

$$
\frac{V_{out}(s)}{V_{in}} = \frac{s^2}{s^2 + s\frac{g_{m2}}{C_2} + \frac{g_{m1}g_{m2}}{C_1C_2}}.
$$

(2.4)

Therefore, the pass-band gain is unity. The design challenge is to ensure that the 3-dB bandwidth is lower than the smallest signal frequency to be detected while the capacitor values are relatively small. To further reduce the bandwidth, $G_{m1}$ and $G_{m2}$ are kept small. The simulated bandwidth is 7.34kHz which is less than the targeted operating range of 13kHz to 25kHz when $C_1$ and $C_2$ are 10pF.
and 1pF, respectively. The simulated output power spectral density at 20kHz is 403.4nV/√Hz.

2.1.4 Band-Pass Filter

The purpose of the band-pass filter is to remove the noise and the interference associated with the signal to be detected. The topology of the band-pass filter is shown in Figure 2.5(a), which consists of four OTAs and four capacitors. The capacitors are provided on-chip. The band-pass filter converts the input signal \( V_{in} \) into a pair of differential output signals. \( V_{ref} \) is a dc biasing voltage which equals to \( V_{b1} \) in Figure 2.4(a). The schematic of the OTA is shown in Figure 2.5 (b).

![Figure 2.5: (a) Circuit schematic of the band-pass filter. (b) Circuit schematic of the OTAs. W\(_{1,2}\) = 0.9µm, W\(_{3,4}\) = 1.5µm, W\(_{5,6}\) = 1µm, W\(_{7}\) = 2.7µm, W\(_{8,9}\) = 8µm, W\(_{10-13}\) = 2µm, W\(_{14-15}\) = 4µm, L\(_{1-7}\) = 7µm, L\(_{8-15}\) = 0.35µm. V\(_{b1}\) = 1.2V, V\(_{b2}\) = 0.5V, V\(_{b3}\) = V\(_{bx}\) = 1.6V.](image-url)
2.5(b), and the topology is taken from [30]. All the biasing voltages are provided off-chip. The common-mode feedback (CMFB) circuitry sets the output dc operating point to $V_{bx}$ and reduces common-mode output voltage fluctuations through negative feedback. The characteristic transfer function of the band-pass filter is,

$$v_{m}^\text{out}(s) = \frac{g_{m1}s}{s^{2} + \frac{g_{m2}}{C_1} + \frac{g_{m3}g_{m4}}{C_1C_2}},$$  \hfill (2.5)\]

and the center frequency and the quality factor are,

$$\omega_o = \sqrt{\frac{g_{m1}g_{m4}}{C_1C_2}},$$  \hfill (2.6)\]

and

$$Q = \frac{g_{m1}}{g_{m2}} \frac{C_1}{C_2}.$$  \hfill (2.7)\]

The design challenge of the band-pass filter is to pinpoint the center frequency within the required operating frequency range without using unreasonably large capacitors while maintaining a good quality factor. According to Equations (2.6) and (2.7), the center frequency can be decreased by reducing $g_{m3}g_{m4}$ and enlarging

Figure 2.6: Simulated frequency response of the band-pass filter at different center frequencies.
C\(_1\)C\(_2\) while the quality factor can be improved by increasing the ratio of C\(_1\) to C\(_2\) and \(g_{m3}\) to \(g_{m2}\). The OTA trans-conductance can be adjusted by varying the biasing voltages and transistor aspect ratios. The transistor sizes shown in Figure 2.5(b) are that of \(g_{m1}\). The transistor sizes in \(g_{m2-4}\) and the biasing voltages are adjusted to achieve the desired center frequency and quality factor where \(g_{m1} = 5g_{m2} = g_{m3} = g_{m4}\). The simulated frequency response at the center frequencies of 12.8kHz, 16.5kHz, 21.1kHz, and 26.8kHz is shown in Figure 2.6. The measured quality factor is approximately 10, where C\(_1\) and C\(_2\) are 10pF and 1pF, respectively. The simulated output power spectral density at 20kHz is simulated to be 89.99 nV/\(\sqrt{Hz}\).

### 2.1.5 Phase-Locked Loop

A type-II voltage-mode PLL is designed, and the circuit schematic is shown in Figure 2.7. A ring-oscillator based VCO is implemented where the oscillating frequency is tunable from 6.66MHz to 14.64MHz as the control voltage varies from rail-to-rail. The output oscillating frequency is reduced by 512 times to the tuning range of 13.02kHz-28.6kHz through 9-cascaded divided-by-2 digital logic circuitry implemented with T flip-flops. The simulated gain of the VCO (\(K_{VCO}\)) is 4.198MHz/V. The phase detector is implemented with D flip-flops. The simulated gain of the charge pump (\(K_{CP}\)) is 275\(\mu\)A/rad. The PLL pull-in time is given by,

\[
T_p = \Delta \omega_0 \frac{NC_1}{K_{VCO} K_{CP} \pi},
\]

(2.8)
where, $\Delta\omega_o$ is the change in input frequency [31]. Therefore, for a 100ms pull-in time and 1kHz frequency hopping, $C_1$ is set to 0.22µF. The loop filter transfer function is given by,

$$
\frac{V_c(s)}{I_{cp}(s)} = \frac{sRC_1 + 1}{s^2RC_1C_2 + s(C_1 + C_2)}.
$$

(2.9)

The zero ($\omega_z$) locates at $1/RC_1$, and relates to the natural frequency ($\omega_n$) and damping ratio ($\zeta$) as,

$$
\zeta = \frac{\omega_n}{2\omega_z},
$$

(2.10)

where, $\omega_n$ is given by,

$$
\omega_n = \frac{K_{VCO}K_{CP}}{NC_1}.
$$

(2.11)

By setting $\zeta$ to 0.7 for optimal damping ratio and settling time, $R$ is calculated to be 5.69kΩ from $\omega_z$. $C_2$ is set to 30% of $C_1$ as a general rule of thumb. $R$, $C_1$ and $C_2$ are off-chip components during chip testing. The simulated PLL parameters are summarized in Table 2.1.
2.1.6 Mixer

The mixer down-converts its input signal to DC by multiplying the local-oscillator (LO) signal and the input signal where the two signals have the same frequency. The schematic of the mixer is shown in Figure 2.8. Unlike Gilbert-cell based mixer topology, the current source at the bottom is removed to increase the headroom at the output. The biasing voltage is provided off-chip. The output power spectral density at 20kHz is simulated to be 77.78 nV/√Hz.

<table>
<thead>
<tr>
<th>Type</th>
<th>Integer-N, Type-II</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reference Frequency</td>
<td>20kHz</td>
</tr>
<tr>
<td>VCO Tuning Range</td>
<td>13.02kHz-28.6kHz</td>
</tr>
<tr>
<td>VCO Phase Noise (12.6MHz Center Freq.)</td>
<td>-101.7dBc/Hz at 10kHz</td>
</tr>
<tr>
<td>Power Consumption</td>
<td>5.22mW</td>
</tr>
</tbody>
</table>
2.1.7 Low-Pass Filter

The low-pass filter after the mixer removes the tone located at $2\omega_o$. The circuit schematic of the low-pass filter is shown in Figure 2.9. The topology is taken from [29], and the schematic of the OTAs is the same as that of the high-pass filter. The transfer function from the input to the output is given by,

$$\frac{V_{out}(s)}{V_{in}} = \frac{\frac{g_{m1}g_{m2}}{C_1C_2}}{s^2 + s\frac{g_{m2}}{C_2} + \frac{g_{m1}g_{m2}}{C_1C_2}}.$$  (2.12)

The pass-band gain is unity, and the bandwidth should be small enough so that the tone at $2\omega_o$ can be effectively removed. The simulated bandwidth of the low-pass filter is 1.434kHz when $C_1$ and $C_2$ are 10pF and 5pF, respectively. Both capacitors are implemented on-chip. The simulated output power spectral density at 20kHz is 81.25 nV/$\sqrt{Hz}$.

![Figure 2.9: Circuit schematic of the low-pass filter.](image)

2.2 Experimental Measurements and Discussion

The designed lock-in amplifier is fabricated in TSMC CMOS 0.35µm technology, and the die photo is shown in Figure 2.10. Only the phototransistor
array is visible in the micrograph as the rest of the chip is covered by metal layer to prevent noise due to interference of optical signals with the circuitry. The optical responsivity of the photo-transistors and the TIA in the visible electromagnetic spectrum are measured. A Xenon arc lamp is used as the white light source. A monochromator is used to control the output light wavelength where a partial spectrum of visible light (470nm to 690nm wavelength) is synthesized. The power of the light is measured by an optical power meter. Figure 2.11 shows the TIA output voltage normalized with respect to the measured optical power as a function of the wavelength. The photo-transistors demonstrate maximum responsivity when they are excited by the orange wavelength ($\lambda = 650$nm), and least responsivity when they are excited by the blue wavelength ($\lambda = 470$nm wavelength). As a result, a blue LED is used in the subsequent measurements to test the robustness of the system. Also, most of the luminescence sensors emit in the wavelength between green and orange wavelength where the system is most responsive [27][28].
The VCO tuning range is measured with respect to the control voltage as shown in Figure 2.12. The frequency tuning range is from 32kHz to 13kHz as the control voltage is swept from rail-to-rail which covers the intended frequency operating range. The PLL phase noise is also measured, and the output spectrum is shown in Figure 2.13, where the phase noise is measured as -58dBc/Hz at 100Hz offset.

A blue LED is used as the input light source and is driven by a function generator at 20kHz. The DC offset voltage used to drive the LED is set to 2.2V, 2.525V, and finally to 2.85V in three steps while maintaining the same AC amplitude such that the average optical power incident on the LIA is increased to
67µW, 75µW, and 82µW, respectively. The measured lock-in amplifier DC output voltages (shown in Figure 2.14) at these optical powers are 1.2V, 1.9V, and 2.6V, respectively.

The lock-in amplifier output voltage versus the input optical power is shown in Figure 2.15 which shows good linearity. The sensitivity is measured to be approximately 100mV/µW (incident optical power). Strong interference is introduced intentionally to the input signal to verify the robustness of the system where the input signal of 20kHz is amplitude-modulated by another signal of 21kHz with 50% modulation depth. The measured output voltage versus the input optical power is shown in Figure 2.15, where a linear relationship is preserved but the sensitivity is reduced to 34mV/µW. The measured relationship when the interference is changed to 100kHz and 50% modulation depth is also shown in Figure 2.15, where the sensitivity is improved to 65mV/µW. It is worth
mentioning that the above measurement is performed with a background ambient room light of 54.3µW power. Therefore, the dynamic reserve or the noise-to-signal ratio at 67µW input optical power can be calculated as \((54.3µW+67µW/2)/67µW\) or 2.35dB, and 1.31dB at 82µW.

In summary, under situations where strong interference is super-imposed on top of the input signal, the output versus input relationship still demonstrates good
linearity and good sensitivity. The measured performance of the LIA is summarized in Table 2.2. Table 2.3 compares the measured performance between the proposed LIA and designs from other groups.

Table 2.2: Lock-in amplifier performance summary

<table>
<thead>
<tr>
<th>Technology</th>
<th>TSMC CMOS 0.35μm</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dynamic Reserve</td>
<td>1.31dB minimum</td>
</tr>
<tr>
<td>Frequency Tuning Range</td>
<td>13kHz - 25kHz</td>
</tr>
<tr>
<td>Sensitivity</td>
<td>34mV/μW minimum</td>
</tr>
<tr>
<td>Chip Area</td>
<td>1.5mm × 1mm (pads not included)</td>
</tr>
<tr>
<td>Power Consumption</td>
<td>12.79mW</td>
</tr>
</tbody>
</table>

Table 2.3: Comparison with existing designs

<table>
<thead>
<tr>
<th>Frequency</th>
<th>Technology</th>
<th>Power</th>
<th>Input Signal Level</th>
<th>Output Dynamic Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>[18] 1.5kHz</td>
<td>-</td>
<td>-</td>
<td>50mV</td>
<td>0.1V-1V</td>
</tr>
<tr>
<td>[20] 100Hz</td>
<td>CMOS 0.35μm</td>
<td>-</td>
<td>0.35-52.17μV</td>
<td>2.8mV-98.4mV</td>
</tr>
<tr>
<td>[21] 20kHz</td>
<td>CMOS 0.7μm</td>
<td>25mW</td>
<td>100nV-1μV</td>
<td>0.3-0.55V</td>
</tr>
<tr>
<td>[22] 30kHz</td>
<td>CMOS 0.35μm</td>
<td>110mW</td>
<td>1μV</td>
<td>-0.2V-0.4V</td>
</tr>
<tr>
<td>This Work 13-25kHz</td>
<td>CMOS 0.35μm</td>
<td>12.79mW</td>
<td>(Optical) 500nA-3μA (photo-current)</td>
<td>1.2V-2.85V</td>
</tr>
</tbody>
</table>

2.3 Conclusions

A low-power optoelectronic lock-in amplifier is designed and fabricated in TSMC 0.35μm CMOS technology. The LIA is experimentally tested to examine its optical sensitivity in the visible electromagnetic spectrum. The LIA performance is optimized at 20kHz modulation frequency but the design is also operational in the frequency range from 13kHz to 25kHz. At 20kHz input frequency, the sensitivity of the LIA is 100mV/μW. The LIA has demonstrated good input/output linearity. The described LIA will be useful in the development
of portable optical spectroscopy instrumentation and field-usable optical based biological and chemical sensors.
CHAPTER 3: LC-VCO WITH LINEARIZED FREQUENCY TUNING CHARACTERISTIC

As described in Chapter 1, VCO has a significant impact on the PLL noise performance and frequency tuning range. Integrated LC-VCOs are widely used in modern day wireless transceivers due to their excellent phase noise performance [32]-[34]. The tunable oscillation frequency of a VCO depends on the variable capacitance of the varactors. To date, junction diode varactors and MOS varactors have been integrated on-chip in VCOs as shown in Figure 3.1 [35]. The diode varactor can be implemented using a reverse biased p+/n-well junction [36]. Here, the junction capacitance is given as [37],

$$C = \frac{C_0}{\left(1 + \frac{V_G}{V_B}\right)^M},$$  \hspace{1cm} (3.1)

where, $V_G$ is the reverse biased voltage across the diode varactor. $V_B$ is the junction built-in voltage. $C_0$ is the capacitance subject to zero input voltage. M

---

Figure 3.1: Integrated LC-VCO with (a) diode varactor, (b) inversion-mode MOS varactor, and (c) accumulation-mode MOS varactor.
depends on the junction doping profile [8]. As mentioned in [8], the disadvantages associated with the diode varactor include limited control voltage range due to the required voltage headroom to maintain the reverse biasing condition for the diode, and reduced oscillation frequency tuning range due to the large parasitic capacitance between the n-well and p-substrate.

The other approach to implement an on-chip varactor is to use metal-oxide semiconductor (MOS) field-effect transistors (FETs). Two types of MOS varactors have been implemented, the inversion-mode and accumulation-mode varactors [38]. The inversion-mode varactor is implemented by connecting its source and the drain of a MOSFET together as one capacitor terminal, and using the gate as the other capacitor terminal. Here, the substrate is tied to \( V_{DD} \) and thus the transistor cannot enter the accumulation mode and the frequency tuning range is enlarged [35]. In this case, the operation mode of the transistor changes between the inversion mode and the depletion mode with respect to the voltage variation across the varactor. The accumulation-mode varactor is implemented by using the n-well as one capacitor terminal and the FET gate as the other capacitor terminal. In this case, the operation mode of the transistor changes between the accumulation mode and depletion mode. As the substrate is connected to a variable tuning voltage, the accumulation-mode varactor is more susceptible to latch-up [36]. The transition slope between the maximum and minimum capacitances is steeper for the inversion-mode varactor, so the linear range of the
frequency tuning curve for the VCO with an inversion-mode varactor is not as wide as the VCO with an accumulation-mode varactor.

The transfer function of the VCO output phase with respect to its control voltage can be modeled as,

\[ \frac{\theta_{\text{out}}(s)}{V_{\text{ctrl}}(s)} = \frac{K_{\text{VCO}}}{s} , \]

where, \( K_{\text{VCO}} \) is the gain of the VCO. Ideally, the frequency varies linearly with respect to the control voltage through the entire tuning range, where \( K_{\text{VCO}} \) is modeled as a constant. The nonlinearity introduced through \( K_{\text{VCO}} \) directly translates into the PLL loop dynamics and thus an extra effort is required to model the VCO nonlinear characteristics. In this work, an oscillation frequency linearization technique is proposed which allows a linear oscillation frequency tuning by linearization of the inversion-mode varactor \( C(V) \) response.

### 3.1 Design of Linear Frequency Tuning VCO

The inversion-mode varactor in Figure 3.1(b) is implemented by connecting the source and drain of a MOSEFT as one terminal of a capacitor and using the gate as the other capacitor terminal. A typical \( C(V) \) curve of an inversion-mode PMOS varactor is shown in Figure 3.2(a). The operation mode of the varactor changes between inversion and depletion modes when the voltage difference across the varactor nears the threshold voltage of the transistor [39].
When the gate-source voltage is less than the threshold voltage, the varactor operates in the inversion mode and the varactor capacitance equals to the gate-oxide capacitance of the transistor. When the gate-source voltage exceeds the threshold voltage, the varactor operates in the depletion mode, and the varactor capacitance equals to the series combination of the oxide and depletion capacitances. Due to the highly non-linear C(V) profile of the varactor, the corresponding frequency tuning curve also demonstrates strong non-linear characteristics as shown in Figure 3.2(b).

Figure 3.2: (a) Example C(V) curve of an inversion-mode PMOS varactor. (b) Frequency tuning curve of the LC-VCO with an inversion-mode varactor.
When the tuning voltage is less than 1.2V, the varactor operates in the depletion mode and the oscillation frequency stays constant. The effective capacitance experienced by the oscillation signal over the oscillation cycle does not change and thus the oscillation frequency is invariant with respect to the tuning voltage. When the tuning voltage exceeds 1.2V, the effective capacitance experienced by the oscillation signal equals to the mix of oxide and depletion capacitances, where the oscillation signal drives the varactor into inversion mode for a portion of the oscillation period, and depletion mode for the rest of the period. The higher the tuning voltage, the more time the varactor spends in the inversion mode. Therefore, the effective capacitance increases with respect to the tuning voltage and, thus, the oscillation frequency starts to decrease.

To generate a linear frequency tuning curve, a new varactor configuration is proposed as shown in Figure 3.3. The varactor in Figure 3.1 is broken into a number of varactors $M_1$-$M_N$ with smaller dimensions. While the varactor gates are still connected to the VCO output, the drain-source terminals are separated by resistors such that a resistor network is formed between $V_{DD}$ and the tuning voltage. As a result, the voltage difference between two adjacent gate-source voltages equals to,

$$V_x = \frac{V_{DD} - V_{tune}}{N}. \quad (3.3)$$
The resistors connected with the varactors could lead to degradation of the varactor quality factor which could lead to a reduced quality factor of the LC tank. Therefore, an upper bound on the resistance values is placed by the VCO noise requirement. On the other hand, small resistance values lead to extra power consumption in the series resistor network. Therefore, proper resistance choice is required to compromise with the power consumption versus noise trade-off. At an arbitrary tuning voltage, the intermediate voltages $V_{\text{INT1-INTN}}$ increase by $V_X$ incrementally. When the drain-source voltage of the varactor is increased by $V_X$, the gate voltage required to change the operating mode is also increased by $V_X$. Thus, the varactor $C(V)$ curve of $M_N$ is voltage-shifted by $V_X$ compared to that of $M_{N-1}$. Figure 3.4 shows the voltage-shifted $C(V)$ curves of $M_1$-$M_N$. Since $M_1$-$M_N$ are connected in parallel at the oscillator output, the overall capacitance experienced by the oscillation signal equals to the sum of every individual $C(V)$ curve in Figure 3.4. The overall $C(V)$ curve is shown in Figure 3.5, where the linearity is greatly improved compared to that in Figure 3.2(a).

![Proposed varactor configuration consisting of PMOS varactors and resistor network.](image)

Figure 3.3: Proposed varactor configuration consisting of PMOS varactors and resistor network.
To model the C(V) curve mathematically, the continuous varactor C(V) curve is modeled by a piece-wise linear curve as shown in Figure 3.6, where the continuous transition region from the inversion mode to the depletion mode is modeled by a ramp with a ramp width of $V_w$. Two constant sections with capacitances $C_{\text{max}}$ and $C_{\text{min}}$ are used to model the sections where the capacitance variation is small. Therefore, the slope of the ramp is given by,
At an arbitrary tuning voltage, the gate voltage when the voltage difference across the varactor equals to the threshold voltage is marked as $V_1 + \alpha V_W$, where $\alpha$ is in percentage. The corresponding capacitance at $V_1 + \alpha V_W$ is between $C_{\text{max}}$ and $C_{\text{min}}$. Therefore, the voltage $V_1$, which marks the boundary between the $C_{\text{max}}$ section and the ramp section, is given by,

$$V_1 = V_{\text{tune}} - V_{th} - \alpha V_W.$$  \hfill (3.5)

Similarly, the operating mode of $M_n$ starts to change at $V_n$, where $V_n$ is given by,

$$V_n = V_{\text{tune}} - V_{th} - \alpha V_W + (n-1)V_X.$$  \hfill (3.6)

At $V_Y$, the operating mode of $M_1$-$M_N$ have all changed into the depletion mode, and $V_Y$ exceeds $V_N$ by $V_W$ as,

$$V_Y = V_{\text{tune}} - V_{th} + (1-\alpha)V_W + (N-1)V_X.$$  \hfill (3.7)
By substituting Equation (3.3) into Equation (3.7), \( V_Y \) evaluates to,

\[
V_Y = \frac{V_{\text{tune}}}{N} - V_{th} + (1 - \alpha)V_W + \frac{N - 1}{N} V_D D.
\]  

(3.8)

Therefore, \( V_Y \) weakly depends on the tuning voltage when \( N \) is set to a large value.

Figure 3.7: Overall piece-wise linear C(V) curve.

Any two adjacent C(V) curves are separated by \( V_X \). When \( V_X \) exceeds \( V_W \), a gate voltage interval \( V_X - V_W \) exists where the capacitance of every C(V) curve is either \( C_{\text{max}} \) or \( C_{\text{min}} \) as shown in Figure 3.6. As a result, when the C(V) curves are added, the overall C(V) curve consists of successive ramp sections and constant sections instead of the linear profile shown in Figure 3.5. Therefore, \( V_X \) is set to match \( V_W \) to ensure the linearity of the C(V) profile. When the C(V) curves of \( M_1 - M_N \) are added, the overall C(V) profile also consists of a ramp section and two constant sections as shown in Figure 3.7. The capacitance of the two constant sections equals to \( NC_{\text{max}} \) and \( NC_{\text{min}} \). The slope of the ramp equals to,
The magnitude of the slope is minimum when the tuning voltage is 0V. As the tuning voltage increases, $V_1$ gradually approaches $V_Y$. When the tuning voltage is $V_{DD}$, the voltage difference between $V_Y$ and $V_1$ is reduced to $V_W$. It can be verified that when the tuning voltage is increased to $V_{DD}$, Equation (3.9) evaluates to,

$$k = -\frac{N_{C_{\max}} - N_{C_{\min}}}{V_Y - V_1} = -\frac{N_{C_{\max}} - N_{C_{\min}}}{V_W + \frac{N-1}{N}(V_{DD} - V_{tune})}.$$

The effective capacitance experienced by the oscillation signal over the oscillation period depends on the C(V) profile within the oscillation signal voltage span. As shown in Figure 3.7, the oscillation signal amplitude is bounded by $V_{CM} \pm V_A$ over the oscillation period, where $V_{CM}$ is the common-mode voltage of the oscillation signal. The capacitance traversed by the oscillation signal varies with respect to the tuning voltage, where two different scenarios can be categorized. In the first scenario, the C(V) profile is strictly linear within the oscillation amplitude span as illustrated by the red sections in Figure 3.7. In the second scenario, the oscillation signal traverses both the $N_{C_{\max}}$ section and the linear section as highlighted by the green regions. The boundary which separates the two operating scenarios is when $V_1$ equals to $V_{CM} - V_A$. Based on Equation (3.5), the corresponding tuning voltage evaluates to,
The effective capacitance is evaluated by a time-averaged approach. Though not very accurate, it provides a good indication on how the effective capacitance varies with respect to the tuning voltage. In the first scenario, since the \( C(V) \) profile over the oscillation signal voltage span is linear, the time-averaged capacitance equals to the instantaneous capacitance evaluated at \( V_{CM} \), which evaluates to,

\[
C_{eff_1} = NC_{max} + (V_{CM} - V_1)k
= NC_{max} - (NC_{max} - NC_{min})V_{CM} - V_1/V_{Y} - V_1.
\]

Also, since the oscillation frequency is given by Equation (3.13), the frequency variation with respect to the tuning voltage can be evaluated as that in Equation (3.14).

\[
\omega = \frac{1}{\sqrt{LC_{eff_1}}},
\]

\[
\frac{\partial \omega}{\partial V_{tune}} = \frac{\partial \omega}{\partial V_1} \frac{\partial V_1}{\partial V_{tune}}
= -\frac{(NC_{max} - NC_{min})(V_Y - V_{CM})}{2\sqrt{L}V_Y - V_1 \left( \sqrt{NC_{max}V_Y - (NC_{max} - NC_{min})V_{CM} - NC_{min}V_1} \right)^3}.
\]

Since, \( V_Y \) weakly depends on the tuning voltage, the numerator can be treated as a constant. The denominator consists of a quadratic function with \( V_1 \) as the variable. Since \( V_1 \) linearly depends on the tuning voltage as given by Equation (3.5), Equation (3.14) can be represented as,
\[
\frac{\partial \omega}{\partial \text{V}_{\text{tune}}} \propto -\frac{a}{(b - \text{V}_{\text{tune}})^2}.
\] (3.15)

By integrating Equation (3.15) with respect to \( \text{V}_{\text{tune}} \), the oscillation frequency varies with respect to the tuning voltage as,

\[
\omega \propto \frac{a}{b - \text{V}_{\text{tune}}}.
\] (3.16)

In the second scenario, the oscillation signal traverses two different sections of the C(V) profile. In particular, the percentage time the oscillation signal stays in the NC\(_{\text{max}}\) section is \( V_1 - (V_{\text{CM}} - V_{\text{A}}) \) out of \( 2V_{\text{A}} \), and the percentage time in the linear section is \( V_{\text{CM}} + V_{\text{A}} - V_1 \) out of \( 2V_{\text{A}} \) as indicated in Figure 3.7. Therefore, the effective capacitance is given by,

\[
C_{\text{eff}} = \frac{V_1 - (V_{\text{CM}} - V_{\text{A}})}{2V_{\text{A}}} \cdot \frac{NC_{\text{max}}}{NC_{\text{max}}} + \frac{(V_{\text{CM}} + V_{\text{A}}) - V_1}{2V_{\text{A}}} \left[ \frac{NC_{\text{max}} + (V_{\text{CM}} + V_{\text{A}}) - V_1}{2} \right] \]

\[
= NC_{\text{max}} \frac{(NC_{\text{max}} - NC_{\text{min}})(V_{\text{CM}} + V_{\text{A}} - V_1)^2}{4V_{\text{A}}(V_1 - V_{\text{CM}})}.
\] (3.17)

By substituting Equation (3.17) into Equation (3.13),

\[
\omega = \frac{1}{\sqrt{4LNC_{\text{max}}V_{\text{A}}(V_1 - V_{\text{CM}}) - L(NC_{\text{max}} - NC_{\text{min}})(V_{\text{CM}} + V_{\text{A}} - V_1)^2}}.
\] (3.18)

Since, the denominator consists of a second order polynomial divided by a first order polynomial, the oscillation frequency can be approximated as,

\[
\omega \propto \frac{1}{\sqrt{a - \text{V}_{\text{tune}}}.
\] (3.19)
3.2 Experimental Results and Discussion

A single-switch (SS) LC-VCO is implemented with TSMC 0.18µm CMOS technology as shown in Figure 3.8. The die microphotograph is shown in Figure 3.9, and the chip area is 1.25mm$^2$. The proposed varactor configuration as shown in Figure 3.3 is implemented with 15 PMOS varactors and 15 resistors. The dimension of each varactor is 150µm by 0.18µm and the value of the resistance $R$, is 200Ω. The square integrated inductor is implemented with the top metal layer, where the metal sheet resistance is 0.036Ω/□. The simulated inductance is 4.8nH with a quality factor of 5.1 at 1GHz. The VCO draws 4mA of current from a 1.8V power supply. The measured and simulated frequency tuning curves are shown in Figure 3.10, where the frequency tuning ranges are 9.5% and 8.2%, respectively. The VCO gains of the measured and simulated tuning curves are 37MHz/V and 60MHz/V, respectively. The phase noise measurement is shown in Figure 3.11.

![Figure 3.8: Schematic of the fabricated single-switch (SS) LC-VCO. Transistor sizes: $W_1 = 360\mu m$, $L_1 = 2.7\mu m$, $W_{2,3} = 120\mu m$, $L_{2,3} = 0.3\mu m$.](image-url)
where the phase noise is measured to be -117dBc/Hz at 1MHz frequency offset, and -125dBc/Hz at 3MHz frequency offset. The simulated signal amplitude at 1GHz and the first five harmonics are shown in Figure 3.12. The measured output signal spectrum at 1GHz is shown in Figure 3.12. The VCO performances between similar designs are summarized in Table 3.1.

Figure 3.9: Die microphotograph of the designed SS LC-VCO.

Figure 3.10: Top: Measured SS LC-VCO frequency tuning curve. Bottom: Simulated SS LC-VCO frequency tuning curve.
As mentioned previously, the effective capacitance experienced by the oscillation signal over the oscillation period can be categorized into two scenarios. As a result, the oscillating frequency and the tuning voltage dependency vary between the two scenarios. The tuning voltage which separates the two scenarios is given by Equation (3.11). If $V_{CM}$ equals to $V_{DD}$, $V_A$ is roughly 0.9V, $V_{th}$ is taken as 0.4V, and $\alpha V_W$ is estimated to be 0.1V, then the tuning voltage is

![Image](image1)

**Figure 3.11:** Measurement results of SS LC-VCO phase noise.

![Image](image2)

**Figure 3.12:** Simulated signal amplitude of the fundamental tone at 1GHz and the first five harmonics.

As mentioned previously, the effective capacitance experienced by the oscillation signal over the oscillation period can be categorized into two scenarios. As a result, the oscillating frequency and the tuning voltage dependency vary between the two scenarios. The tuning voltage which separates the two scenarios is given by Equation (3.11). If $V_{CM}$ equals to $V_{DD}$, $V_A$ is roughly 0.9V, $V_{th}$ is taken as 0.4V, and $\alpha V_W$ is estimated to be 0.1V, then the tuning voltage is
calculated to be 1.4V. For the simulated frequency tuning curve in Figure 3.10, the frequency and tuning voltage dependency are separated into two different regions when the tuning voltage reaches 1.2V. When the tuning voltage is less than 1.2V, the tuning curve is linear and the dependency is modeled by Equation (3.16). As the tuning voltage continues to increase, the dependency is modeled by Equation (3.19). Similar results can also be observed in the measured frequency tuning curve.

3.3 Conclusions

A technique to improve the linearity of the oscillation frequency tuning curve for LC-VCO with an inversion-mode varactor is described in this Chapter. The proposed technique improves the frequency tuning curve through linearization of the varactor C(V) characteristics. The designed varactor configuration consists of multiple varactor units, which are connected to the oscillator output at one end,

Figure 3.13: Measured VCO output spectrum.
and a resistor divider network at the other end. The C(V) characteristic of each varactor are voltage shifted by the incremental voltage of the resistor divider network, and the net capacitance at the oscillator output has a more linear C(V) characteristics.

Table 3.1: Performance comparison with other designs

<table>
<thead>
<tr>
<th>Ref.</th>
<th>Technology</th>
<th>Center Frequency</th>
<th>Tuning Range</th>
<th>Phase Noise</th>
<th>Power Consumption</th>
<th>FoM</th>
</tr>
</thead>
<tbody>
<tr>
<td>[40]</td>
<td>0.35µm BiCMOS</td>
<td>5.7GHz</td>
<td>8.8%</td>
<td>-116dBc/Hz @ 1MHz</td>
<td>3.4mA from 3V</td>
<td>181dB</td>
</tr>
<tr>
<td>[41]</td>
<td>0.25µm CMOS</td>
<td>2.4GHz</td>
<td>11%</td>
<td>-115.7dBc/Hz @ 600kHz</td>
<td>6mA from 2.5V</td>
<td>176dB</td>
</tr>
<tr>
<td>[42]</td>
<td>0.13µm CMOS</td>
<td>2.4GHz</td>
<td>4%</td>
<td>-126dBc/Hz @ 3MHz</td>
<td>2.68mA from 1.2V</td>
<td>179dB</td>
</tr>
<tr>
<td>[43]</td>
<td>0.15µm CMOS</td>
<td>4.5GHz</td>
<td>17%</td>
<td>-109dBc/Hz @ 1MHz</td>
<td>4mA from 1.5V</td>
<td>174dB</td>
</tr>
<tr>
<td>[44]</td>
<td>0.12µm CMOS</td>
<td>10GHz</td>
<td>17%</td>
<td>-117.7dBc/Hz @ 1MHz</td>
<td>0.8V</td>
<td>-</td>
</tr>
<tr>
<td>This work</td>
<td>0.18µm CMOS</td>
<td>1.05GHz</td>
<td>9.5%</td>
<td>-125dBc/Hz @ 3MHz</td>
<td>4mA from 1.8V</td>
<td>170dB</td>
</tr>
</tbody>
</table>
CHAPTER 4: TIME-WEIGHTED OSCILLATING FREQUENCY MODEL FOR LC-VCO WITH IMPROVED PHASE NOISE PERFORMANCE

In this Chapter, the oscillating frequency tuning model and the phase noise improvement issues of LC-VCO are examined more closely. As previously mentioned, integrated LC-VCOs as shown in Figure 4.1(a) are widely used in modern wireless transceivers due to their superior phase noise performance as opposed to their counterparts such as the ring oscillators. Noises associated with the active and passive components are converted into the phase noise through different mechanisms, which are well summarized by Rael and Abidi [45]. In particular, two different sources have profound contributions to the phase noise performance. The first source is the flicker noise associated with the tail biasing transistor. This low-frequency noise enters the resonator as the amplitude-modulated (AM) noise, which is then converted into the phase-modulated (PM) noise through the varactor. The second source is the thermal noise of the tail biasing transistor at twice of the oscillation frequency $2\omega$, which is down-converted to the close-in phase noise of the carrier through the interaction with the carrier. Different techniques have been proposed to reduce the incurred phase noise due to both sources. To reduce the impact of the low-frequency flicker noise, one method is to reduce the varactor sensitivity with respect to the AM noise through a new varactor configuration as described by Bonfanti et al. [46].

To reduce the thermal noise of the tail transistor at $2\omega$, the filter technique in
Hegazi et al. [17] is proposed, where high impedance with a resonant frequency of $2\omega$ is added between the tail transistor and the LC tank.

The novelty of the current work is twofold. First, a low-power LC-VCO is designed where the impact of both sources of phase noise are reduced simultaneously. Instead of adding the high impedance at $2\omega$ as proposed in [17], a 2nd order RLC notch filter is connected between the tail biasing transistor and the LC tank to suppress the noise power at $2\omega$ as shown in Figure 4.1(b). To reduce the impact of the tail transistor flicker noise up-conversion, passive capacitors are added with the varactor in parallel as designed in [47]. In this paper, a new varactor configuration with the addition of a capacitor divider network is designed to decrease the strength of the AM-to-PM noise conversion as shown in Figure 4.1.
1(b). Capacitor $C_2$ provides an extra path to partially filter the AM noise entering the varactor. Further, we develop a new model for the LC-VCO oscillation frequency based on a new time-weighed approach. Since, it is difficult to make the on-chip spiral inductor tunable, the variation in the oscillation frequency comes from the tunable capacitance of the varactor. The instantaneous capacitance experienced by the oscillating signal varies from one time instance to another; hence, the effective capacitance experienced by the oscillating signal over an oscillation period cannot be accurately represented by the $C(V)$ characteristics of the varactor. Instead, the effective capacitance needs to represent the contribution of the instantaneous capacitance at each time instance within the oscillation period. Therefore, the challenge faced in modeling the oscillation frequency is to model the effective capacitance, which depends on the tuning voltage, the oscillating amplitude, and the $C(V)$ characteristics of the varactor. The effective capacitance is modeled in several previous studies such as in references [36][48][49]. Though accurate, these models have not accounted for the gate-source and gate-drain capacitance associated with the switching transistors. Also, the $C(V)$ profile is approximated by a step function, and a more accurate model for the $C(V)$ profile could lead to more accurate prediction of the oscillation frequency. Therefore, in this work, a new model for the oscillation frequency based on a time-weighted approach is proposed. The $C(V)$ curve is modeled by a piece-wise linear profile consisting of three linear sections. The modeled effective capacitance accounts for both the varactor capacitance, and the oxide capacitance of the switching transistors. Based on the developed model, it is
quantitatively shown that due to the capacitor divider network, the sensitivity of the effective capacitance variation with respect to the AM noise of the tail transistor is reduced, which leads to the improved phase noise performance.

4.1 VCO Design

The proposed VCO design is based on the top-biased double-switch structure. Since the oscillating amplitude of the double-switch LC-VCO is twice as much as compared to its single-switch counterpart for the same biasing current [50], the phase noise performance of the double-switch LC-VCO is better in the current-limited operating regime, and more suitable for low-power applications. The length of the biasing transistor is increased well beyond the minimum length to reduce its flicker noise power. The transistor width is increased accordingly to maintain the same aspect ratio. The transconductance of $M_{2,5}$ needs to be large enough to compensate for the resistance loss of the on-chip integrated inductor. Therefore, a lower bound is placed on the minimum required transistor aspect ratio. On the other hand, the gate-source and the gate-drain capacitance of $M_{2,5}$ affect the oscillation frequency. Large transistor oxide capacitance limits the frequency tuning range, which places an upper bound on the aspect ratio. Also, the thermal noise of $M_{2,5}$ contributes to the phase noise where the phase noise is independent of the transistor sizes [17][51]. Therefore, the transistor lengths are reduced to the minimum length such that the transistor width can also be kept to the minimum in order to reduce the oxide capacitance while the aspect ratio can still provide the sufficient negative resistance to sustain the oscillation.
The relative transistor size ratio between $M_{2,3}$ and $M_{4,5}$ also affects the common-mode voltage of the oscillating signal. In the current-limited operating regime, the oscillating amplitude increases linearly with respect to the biasing current. The oscillating amplitude is bounded by the analog ground at the peak, and the ground rail at the trough. As the oscillating amplitude gradually approaches the two boundaries, it starts to saturate and becomes independent of the biasing current, and the oscillator enters the voltage-limited operating regime. Therefore, the oscillating amplitude should be biased at the boundary between the current-limited and the voltage-limited operating regime for optimal phase noise performance [52] and the phase noise performance improves as the signal power increases [53]. Intuitively, the common-mode voltage of the oscillating signal should be placed at the middle between the analog ground and the ground rail such that the equal amplitude spans are maximized in both directions. This can be easily achieved by matching the transconductance of $M_{2,3}$ to $M_{4,5}$. This requires that $W_{2,3}$ should be two or three times larger than $W_{4,5}$ in order to compensate for the body effect experienced by $M_{2,3}$, and the majority carrier mobility difference between the PMOS and NMOS devices. Note that the matching of the transconductance is based on hand analysis while PVT changes can lead to unpredictable common-mode voltage variation.

The variation in the oscillating frequency depends on the tunable capacitance of the varactor. The proposed varactor structure in Figure 4.1(b) consists of
passive capacitors and inversion-mode PMOS varactor. A capacitor divider network consisting of $C_{1-3}$ is added to reduce the flicker noise up-conversion effect due to the presence of the varactor. Therefore, the instantaneous effective capacitance in parallel with the inductor is,

$$C_{eff} = (C_1 + C_2 + C_{var}) || C_s + 4 \left( C_{g_{sd2}} + C_{g_{sd4}} \right) + C_{gs2} + C_{gs4}. \quad (4.1)$$

Also, digital switches controlled by $V_{C1-2}$ are added to extend the frequency tuning range.

### 4.2 Frequency Estimation based on the Time-Weighted Approach

An accurate snapshot of the instantaneous oscillating frequency of the LC-tank based oscillator is given by,

$$\omega = \frac{1}{\sqrt{LC_{eff}}} \sqrt{1 - \frac{R_s^2 C_{eff}}{L}}, \quad (4.2)$$

where, $R_s$ is the series resistance associated with the tank inductor. On one hand, Equation (4.2) can accurately model the oscillation frequency of the LC oscillator with the passive capacitor since the effective capacitance remains constant over the oscillating cycle and thus the instantaneous oscillation frequency is invariant with respect to time. On the other hand, to predict the oscillation frequency of a varactor-based oscillator with Equation (4.2), the effective capacitance which accounts for the capacitance variation over the entire oscillating cycle must be modeled and used in the calculation such that the varactor-based oscillator can be treated as an inductor oscillating with a passive capacitor with the modeled effective capacitance.
In references [48] and [49], the closed-form expressions of the effective capacitance are provided by balancing the inductor and the capacitor current where the harmonics are accounted. Since the proposed expressions of the effective capacitance has not modeled the oxide capacitance associated with the switching transistors, a new approach is proposed in this work to model the effective capacitance experienced by the oscillating signal over an oscillation period, where both the varactor capacitance, and the gate-source and gate-drain capacitances of the switching transistors are accounted. We will later show that the calculated oscillation frequency based on the modeled effective capacitance is in good agreement with the simulation results.

The inversion-mode PMOS varactor capacitance variations with respect to the gate voltage variations at five different tuning voltages are shown in Figure 4.2.

![Figure 4.2 Simulated C(V) characteristics of the PMOS varactor at five different tuning voltages.](image)
Over a single oscillating period, the oscillating signal amplitude spans over a different portion of the C(V) curve, which translates into the variation of the oscillation frequency. For example, when the tuning voltage is at 1.8V, the oscillating signal sweeps the portion of the C(V) curve with the maximum capacitance values, which leads to the lowest oscillation frequency. On the other hand, the oscillating signal sweeps the portion of the C(V) curve with the minimum capacitance values, which leads to the highest oscillation frequency when the tuning voltage is at 0V.

At different tuning voltages, the ease to estimate the effective capacitance over an oscillating period depends on the linearity of the C(V) profile at that tuning voltage. On one hand, at the tuning voltages of 0V and 1.8V, the effective capacitance can be modeled by averaging the varactor capacitance values over the voltage span of the oscillating signal, and the instantaneous oscillation frequency at any time instant within the oscillating period is the same. On the other hand, a much more nonlinear C(V) profile is experienced by the oscillating signal when the tuning voltage is at 0.9V. Since the varactor capacitance at every time instance differs from one another, the instantaneous oscillation frequency varies from time to time. To model the effective capacitance for the nonlinear C(V) profile, averaging the varactor capacitance over the voltage span of the oscillating signal leads to inaccurate results due to the sinusoidal nature of the oscillating signal waveform. As shown in Figure 4.3, for the same incremental change in the voltage \( \Delta V_1 \) and \( \Delta V_2 \), the associated time intervals \( \Delta T_1 \) and \( \Delta T_2 \) differ from each
other. Due to the differences in the time intervals, the varactor capacitance accumulated within the same voltage increment $\Delta V$ varies since the oscillating signal sweeps different portions of the $C(V)$ curve at different paces. For example, the oscillating signal spends more time in section $\Delta V_1$ of the $C(V)$ curve than in section $\Delta V_2$. Therefore, the accumulated capacitance within $\Delta V_1$ will be larger than that in $\Delta V_2$ since both the capacitance values and the corresponding time intervals are greater. This capacitance-time dependency has been taken into account in modeling the effective capacitance, where the contribution of each varactor capacitance segment to the effective capacitance over an oscillating cycle has been weighted based on the time duration the oscillating signal spent within that segment.

![Figure 4.3: The capacitance-time dependency effect experienced by the oscillating signal.](image)

The accuracy of the time-weighted approach is first verified with experimental data. At each tuning voltage, the varactor capacitance over the oscillating signal amplitude as highlighted by the black portions of the $C(V)$ curve in Figure 4.2 is simulated. Then, the $C(V)$ curve is evenly divided into $N$ sections as shown in Figure 4.3, where there is a one-to-one mapping between the capacitance $C_N$ and the oscillating signal voltage $V_N$. Each $V_N$ corresponds to a time instance, $T_N$. The percentage of the time interval $\Delta T_N$ weighted within the oscillating period is calculated by,

$$\Delta T_N \% = \frac{\cos^{-1} V_{N+1} - \cos^{-1} V_N}{2\pi}.$$  (4.3)

The percentage matrix $\Delta T_N \%$ is then multiplied by the capacitance matrix $C_{1:N}$ to ensure that the contribution of the different portions of the $C(V)$ curve is weighted based on the magnitude of the time intervals $\Delta T_N$. Then, all the entries of the product matrix are added, and the sum represents the effective varactor capacitance over an oscillating cycle.

The effective gate-source and gate-drain capacitances over an oscillating cycle have been modeled in a similar way. The oscillating amplitude of the typical LC-VCO can drive the switching transistors into the deep triode region for almost half of the oscillating cycle, and the cut-off state for the other half with a small time period in the saturation region in between as shown in Figure 4.4. The gate-source and gate-drain capacitances of the MOS transistors are modeled by Equations (4.4) and (4.5). In the saturation region,
and in the triode region,

$$C_{gs} = C_{gd} = \frac{1}{2} C_{ox} WL.$$  \hspace{1cm} (4.5)

The time interval, $T_{sat}$, where both the PMOS and the NMOS transistors are in the saturation region is approximated based on $T_2$, where $T_2$ is the time instance when the differential signal voltage equals to the transistor threshold voltage as,

$$-2V_A \cos(\omega T_2) = V_{th},$$  \hspace{1cm} (4.6)

and $T_{sat}$ is given by,

$$T_{sat} = 2 \left( T_2 - \frac{T}{4} \right) = \frac{2}{\omega} \cos^{-1} \left( -\frac{V_{th}}{2V_A} \right) - \frac{T}{2},$$  \hspace{1cm} (4.7)

where, $T$ is the oscillating signal period. As a result, the percentage of the time interval with respect to the oscillating period where both the transistors are in the saturation region is $2T_{sat}$ divided by $T$. The effective gate-source capacitance over an oscillating cycle is then given by,
\[
\frac{2T_{\text{sat}}}{T} \left( \frac{2}{3} C_{\text{ox}} W L \right) + \frac{T - 2T_{\text{sat}}}{2T} \left( \frac{1}{2} C_{\text{ox}} W L \right),
\]

and the effective gate-drain capacitance over an oscillating cycle is given by,

\[
\frac{T - 2T_{\text{sat}}}{2T} \left( \frac{1}{2} C_{\text{ox}} W L \right).
\]

The varactor capacitance, gate-source, and gate-drain capacitances of the switching transistors are substituted into Equation (4.1) to calculate the effective capacitance, which is then substituted into Equation (4.2) to calculate the oscillation frequency.

The comparison of the frequency tuning curve between the calculated frequency and simulated frequency is shown in Figure 4.5, where the calculated frequency tuning curve has preserved the geometric characteristic of the simulated curve with numerical differences. The error in percentage is also shown in Figure 4.5, where the error is less than 1% in general. As a result, the time-weighted approach is an effective method to model the oscillating frequency of a general LC-VCO. The described process of modeling the oscillating frequency heavily depends on the characteristics of the varactor C(V) profile, where the varactor capacitance over the oscillating signal voltage span at every tuning voltage of interest must be simulated in order to predict the oscillating frequency. To reduce the effort required to model the frequency tuning curve, the non-linear varactor C(V) profile is modeled by a piece-wise linear C(V) profile as shown in Figure 4.6. The linear profile consists of two constant sections with capacitance values of \(C_{\text{max}}\) and \(C_{\text{min}}\), and a ramp section with the ramp width \(V_W\). The values of \(V_W\),
$C_{\text{max}}$ and $C_{\text{min}}$ need to be estimated from the simulated C(V) curve. The slope of the ramp $k$ is given by,

$$k = \frac{C_{\text{max}} - C_{\text{min}}}{V_w}.$$  \hspace{1cm} (4.10)

For the continuous C(V) profile, the oscillating signal sweeps a different portion of the C(V) curve at different tuning voltages. Similarly, for the piece-wise linear C(V) profile, depending on the tuning voltages, the oscillating signal amplitude spans over one or multiple sections of the linear C(V) profile, where five different regions of operations can be categorized.
In the first region, the oscillating signal amplitude only sweeps the $C_{\text{min}}$ section of the C(V) curve as illustrated in Figure 4.7. When the tuning voltage is at 0V, the oscillating signal is far from the ramp section. As the tuning voltage increases, the oscillating signal gradually approaches the ramp section until it reaches the boundary between the $C_{\text{min}}$ and the ramp section at a certain tuning voltage $V_1$ as shown in Figure 4.7. $V_1$ is determined based on the assumption that the varactor capacitance equals to $C_X$ (where $C_X$ is between $C_{\text{max}}$ and $C_{\text{min}}$) when the voltage difference across the varactor equals to the transistor threshold voltage. This is a reasonable assumption since the threshold voltage marks the boundary of the transistor operating modes between the inversion mode and the depletion mode [39]. At $C_X$, the corresponding gate voltage is within $V_W$, and its location is indicated by $\alpha V_W$. The unit of $\alpha$ is percentage, and its value also needs to be estimated from the simulated C(V) curve. When the gate voltage of the 

![Figure 4.6: The piece-wise linear C(V) profile used to model the continuous C(V) curve.](image)
varactor equals to $V_{CM} - V_A - \alpha V_W$ (where, $V_{CM}$ is the common-mode voltage of the oscillating signal), the corresponding varactor capacitance is $C_X$. Here, the voltage difference between the gate voltage and tuning voltage is the transistor threshold voltage. Therefore,

$$V_i = V_{CM} - V_A - \alpha V_W + V_m.$$  \hspace{1cm} (4.11)

It should be noted that $V_A$ represents the oscillating amplitude across the varactor, and is different from the oscillating amplitude across the inductor due to the capacitor divider network. The effective varactor capacitance over the oscillating cycle is given by,

$$C_{var1} = \int_0^{2\pi} C_{min} d\theta = C_{min},$$  \hspace{1cm} (4.12)

where the capacitance is independent of the tuning voltage.
In the second operating region, as the tuning voltage continues to increase, the oscillating signal enters the ramp section until it reaches the boundary between the \( C_{\text{max}} \) and the ramp section at a certain tuning voltage \( V_2 \) as shown in Figure 4.8. \( V_2 \) can be determined by noticing that \( V_2 \) exceeds \( V_1 \) by \( V_W \) as shown in Figure 4.7 and Figure 4.8. Therefore,

\[
V_2 = V_{CM} - V_A + (1 - \alpha) V_W + V_{HF}. \tag{4.13}
\]

At \( V_2 \), when the phase of the oscillating signal at the boundary between the \( C_{\text{max}} \) and ramp section is considered as zero, the phase which corresponds to the varactor gate voltage at the boundary between the \( C_{\text{min}} \) and ramp section is denoted as \( \theta_1 \). As a result, the time percentage of the oscillating signal spent in the ramp section over an oscillating period is \( 2\theta_1 \) out of \( 2\pi \) while the time percentage in the \( C_{\text{min}} \) section is \( 2\pi - 2\theta_1 \) out of \( 2\pi \). As the tuning voltage increases beyond \( V_1 \),

![Figure 4.8: The oscillating signal spans within the ramp and the \( C_{\text{min}} \) sections when the tuning voltage is between \( V_1 \) and \( V_2 \).](image-url)
the oscillating signal enters the ramp section, and $\theta_1$ gradually moves away from zero phase. The magnitude of the extra tuning voltage above $V_1$ is related to $\theta_1$ by,

$$V_A \cos \theta_1 = V_A - (V_{min} - V_1).$$

Therefore,

$$\theta_1 = \cos^{-1} \frac{V_A - (V_{min} - V_1)}{V_A}.$$ 

(4.15)

When the tuning voltage is $V_1$, $\theta_1$ evaluates to zero which indicates that $\theta_1$ coincides with the zero phase. At an arbitrary tuning voltage between $V_1$ and $V_2$, the instantaneous capacitance experienced by the oscillating signal at an arbitrary phase $\theta$ between phase zero and $\theta_1$ is determined by considering the magnitude of the phase difference between $\theta$ and $\theta_1$ as,

$$C_{min} + KV_A (\cos \theta - \cos \theta_1).$$

(4.16)

It can be verified that when $\theta$ is zero and the tuning voltages are $V_1$ and $V_2$, Equation (4.16) evaluates to $C_{min}$ and $C_{max}$ respectively as expected. The effective varactor capacitance over an oscillating cycle is evaluated by integrating (4.16) over the appropriate phase intervals as,

$$\int_{\theta_1}^{2\pi - \theta_1} C_{min} d\theta + 2\int_{0}^{\theta} C_{min} + kV_A (\cos \theta - \cos \theta_1) d\theta$$

(4.17)

$$\frac{2\pi}{2\pi - \theta_1},$$

where, the two integrals represent the effective varactor capacitance accumulated within $C_{min}$ and the ramp section, respectively. The above expression evaluates to,

$$C_{var} = C_{min} + \frac{kV_A}{\pi} (\sin \theta_1 - \theta_1 \cos \theta_1).$$

(4.18)
When the tuning voltage equals to $V_1$, Equation (4.18) evaluates to $C_{\min}$ as expected.

In the third operating region, the oscillating signal spans within all three sections of the $C(V)$ curve as illustrated in Figure 4.9(a). The time percentages of the oscillating signal spent in the $C_{\min}$ and the $C_{\max}$ sections are $2\pi - 2\theta_1$ and $2\theta_2$ out of $2\pi$, respectively. The time percentage in the ramp section is $2(\theta_1 - \theta_2)$ out of $2\pi$. $\theta_2$ is determined similarly as $\theta_1$ by considering the magnitude of the extra tuning voltage above $V_2$ as,

$$\theta_2 = \cos^{-1} \frac{V_A - (V_{\text{tune}} - V_2)}{V_A}.$$  (4.19)

When the tuning voltage is $V_2$, $\theta_2$ evaluates to zero which indicates that $\theta_2$ coincides with zero phase as illustrated in Figure 4.8. When the tuning voltage is $V_3$, the oscillating signal reaches the boundary between the $C_{\max}$ and the ramp section as shown in Figure 4.9(b), where $\theta_1$ evaluates to $\pi$. $V_3$ is determined in

![Figure 4.9: The oscillating signal spans within all three sections when (a) the tuning voltage is between $V_2$ and $V_3$ and (b) the tuning voltage is $V_3$.](image)
similar way as $V_1$ and $V_2$ by noticing that the varactor gate voltage is $V_{CM} + V_A - \alpha V_W$ when the corresponding capacitance is $C_X$. Therefore,

$$V_3 = V_{CM} + V_A - \alpha V_W + V_{TH}. \quad (4.20)$$

Another way to determine $V_3$ is by noticing that $V_3$ exceeds $V_1$ by $2V_A$ as shown in Figure 4.7 and Figure 4.9(b). The effective varactor capacitance is determined by integrating the instantaneous capacitance over the oscillating period as,

$$\frac{2\int_0^{\theta_1} C_{\text{max}} d\theta + \int_{\theta_1}^{2\pi - \theta_1} C_{\text{min}} d\theta + 2\int_{\theta_1}^{\theta_2} C_{\text{min}} + kV_A (\cos \theta - \cos \theta_1) d\theta}{2\pi}, \quad (4.21)$$

where, the three integrals represent the varactor capacitance in the $C_{\text{max}}, C_{\text{min}},$ and the ramp section. The above expression evaluates to,

$$C_{\text{var}3} = C_{\text{min}} + \frac{(C_{\text{max}} - C_{\text{min}})}{\pi} \theta_1 + \frac{kV_A}{\pi} (\sin \theta_1 - \sin \theta_1) - \frac{kV_A}{\pi} (\theta_1 - \theta_2) \cos \theta_1. \quad (4.22)$$

In the fourth operating region, the oscillating signal gradually pulls away from the ramp section until it reaches the boundary between the $C_{\text{max}}$ and the ramp section at the tuning voltage $V_4$ as shown in Figure 4.10. By comparing Figure 4.9(b) and Figure 4.10, it is noticed that $V_4$ exceeds $V_3$ by $V_W$ thus,

$$V_4 = V_{CM} + V_A + (1 - \alpha) V_W + V_{TH}, \quad (4.23)$$

where, $\theta_2$ evaluates to $\pi$ at $V_4$. The oscillating signal spends $2\pi - 2\theta_2$ out of $2\pi$ percent of the time in the ramp section, and $2\theta_2$ out of $2\pi$ percent of the time in the $C_{\text{max}}$ section. The effective capacitance is determined by,

$$\frac{2\int_0^{\theta_2} C_{\text{max}} d\theta + \int_{\theta_2}^{2\pi - \theta_2} C_{\text{max}} - kV_A (\cos \theta - \cos \theta_2) d\theta}{2\pi}. \quad (4.24)$$
The expression evaluates to,
\[
C_{\text{var}4} = C_{\text{max}} - \frac{kV_4}{\pi} (\theta_2 \cos \theta_2 - \sin \theta_2 - \pi \cos \theta_2).
\] (4.25)

At \(V_4\), the effective varactor capacitance evaluates to \(C_{\text{max}}\).

In the last operating region, the oscillating signal spans within the \(C_{\text{max}}\) section only, and the effective varactor capacitance evaluates to,
\[
C_{\text{var}5} = \int_0^{2\pi} \frac{C_{\text{max}} d\theta}{2\pi} = C_{\text{max}}.
\] (4.26)

The values of \(V_{1-4}\) are calculated with an iterative approach due to the presence of the varactor body effect and the oscillating signal amplitude variation with respect to the oscillating frequency. Since the source and drain voltages of the PMOS varactor are tied together, the transistor threshold voltage varies with

![Figure 4.10: The oscillating signal spans within the \(C_{\text{max}}\) section when the tuning voltage exceeds \(V_4\).](image-url)
respect to the tuning voltage. This non-ideality is modeled by the well-known second-order body effect expression,

\[ V_{TH} = V_{TH0} + \gamma \left( \sqrt{2\Phi_F + (V_{tune} - V_{DD})} - \sqrt{2\Phi_F} \right). \]  (4.27)

Also, the oscillating amplitude \( V_A \) depends on the oscillation frequency, which depends on the tuning voltage. A linear approximation of the amplitude variation is used in the calculation, where the exact maximum and minimum oscillating amplitudes (\( V_{\text{max}} \) and \( V_{\text{min}} \)) are obtained from the simulation results at the two extremes of the tuning voltages. At an arbitrary tuning voltage, \( V_A \) is given by,

\[ V_A = V_{\text{max}} - \left( \frac{V_{\text{max}} - V_{\text{min}}}{V_{DD}} \right) V_{tune}. \]  (4.28)

When the tuning voltage equals to zero and \( V_{DD} \), \( V_A \) evaluates to \( V_{\text{max}} \) and \( V_{\text{min}} \), respectively. Therefore, to calculate \( V_1 \), it needs to satisfy Equations (4.11) (4.27)(4.28) simultaneously. This is achieved through an iterative approach where an initial guess of the tuning voltage is used in the calculation. Based on the differences in the calculated threshold voltage between Equations (4.11) and (4.27), the tuning voltage is adjusted accordingly until the difference between the calculated threshold voltages is negligible.

The effective varactor capacitance \( C_{\text{var1}} \) to \( C_{\text{var5}} \) is calculated and substituted into Equation (4.1) to calculate the effective capacitance. Then, the oscillation frequency is calculated with Equation (4.2). The comparison between the calculated and the simulated frequency tuning curve is shown in Figure 4.11. The errors in percentage are also shown in Figure 4.11, where the maximum error is at
2%. The main source of the discrepancy is the inaccuracy in modeling the continuous C(V) curve with the piece-wise linear C(V) curve. For example, between \(V_1\) and \(V_2\), the varactor capacitance is over-estimated, which leads to lower calculated oscillating frequency compared with the simulated frequency. Also, between \(V_3\) and \(V_4\), the varactor capacitance is under-estimated, which leads to higher calculated oscillation frequency compared with the simulated frequency.

![Figure 4.11](image)

Figure 4.11: Top: The calculated and the simulated frequency tuning curves based on the piece-wise linear C(V) curve and the time-weighted approach. Bottom: Error in percentage.
4.3 Phase Noise Reduction through the Capacitor Divider Network

The low-frequency flicker noise of the tail biasing current is up-converted into the AM noise by the hard-switching action of the oscillating signal as in a mixer [45][54]. The AM noise is then converted into PM noise through the varactor. The phase noise due to the AM-to-PM conversion mechanism is quantified in reference [46] as,

\[ L(\omega) = \frac{K^2_{AM-FM} S_{AM}(\omega_m)}{2\omega_m^2}. \]  

(4.29)

\( S_{AM} \) is the power spectral density of the amplitude noise, and is given in reference [8] as,

\[ S_{AM}(\omega_m) = \left( \frac{\partial V_A}{\partial I} \right)^2 S_I(\omega), \]  

(4.30)

where, \( S_I \) is the power spectral density of the low-frequency flicker noise. For a standard VCO as shown in Figure 4.1(a), the varactor directly connects to the oscillator output. The oscillating amplitude is proportional to the biasing current derived in reference [8] as,

\[ V_A = \frac{2}{\pi} I R_p, \]  

(4.31)

and

\[ \left( \frac{\partial V_A}{\partial I} \right)^2 = \left( \frac{2}{\pi} R_p \right)^2, \]  

(4.32)

where, \( R_p \) is the equivalent parallel resistance associated with the inductor. With the addition of the capacitor divider network, the varactor is decoupled from the
oscillator output, where the oscillating amplitude at the varactor gate is reduced to,

\[ V_A = \frac{2}{\pi} IR_p \left( \frac{C_3}{C_1 + C_2 + C_3 + C_{\text{var}}} \right) \]  

(4.33)

thus,

\[ \left( \frac{\partial V_A}{\partial I} \right)^2 = \left( \frac{2}{\pi} R_p \right)^2 \left( \frac{C_3}{C_1 + C_2 + C_3 + C_{\text{var}}} \right)^2 \]  

(4.34)

Therefore, compared to Equation (4.32), the oscillator amplitude variation due to the changes in the biasing current is greatly reduced, which leads to the reduced flicker noise power entering the varactor and up-converting into phase noise.

\[ K_{\text{AM-FM}} \] is the sensitivity measurement of the oscillating frequency variation with respect to the oscillating amplitude variation, and is expressed in reference [8] as,

\[ K_{\text{AM-FM}} = \frac{\partial \omega}{\partial V_A} \]  

(4.35)

This derivative is evaluated by multiplying three partial derivatives as,

\[ K_{\text{AM-FM}} = \frac{\partial \omega}{\partial C_{\text{eff}}} \frac{\partial C_{\text{eff}}}{\partial C_{\text{var}}} \frac{\partial C_{\text{var}}}{\partial V_A} \]  

(4.36)

The first partial derivative is evaluated by differentiating Equation (4.2) with respect to \( C_{\text{eff}} \), which evaluates to,

\[ \frac{\partial \omega}{\partial C_{\text{eff}}} = -\frac{1}{2C_{\text{eff}} \sqrt{L C_{\text{eff}} - R_s^2 C_{\text{eff}}^2}} \]  

(4.37)
The second partial derivative measures the sensitivity of the effective capacitance variation with respect to the varactor capacitance variation. It is evaluated by differentiating Equation (4.1) with respect to \( C_{\text{var}} \), which evaluates to,

\[
\frac{\partial C_{\text{eff}}}{\partial C_{\text{var}}} = \frac{C_3^2}{(C_1 + C_2 + C_3 + C_{\text{var}})^2}.
\]  

(4.38)

On the other hand, the instantaneous effective capacitance of the VCO in Figure 4.1 (a) is given by,

\[
C_{\text{eff}} = C_{\text{var}} + 4(C_{g'd2} + C_{g'd4}) + C_{g'2} + C_{g'4},
\]  

(4.39)

and the second partial derivative evaluates to,

\[
\frac{\partial C_{\text{eff}}}{\partial C_{\text{var}}} = 1.
\]  

(4.40)

By comparing Equation (4.38) to (4.40), it is evident that the sensitivity of the effective capacitance variation with respect to the varactor capacitance variation is greatly reduced with the addition of the capacitor divider network, and this leads to reduced \( K_{\text{AM-FM}} \) magnitude and reduced AM noise up-converted into PM noise.

The third partial derivative measures the sensitivity of the varactor capacitance variation with respect to the oscillating signal amplitude variation. It is evaluated by differentiating \( C_{\text{var}1} \) to \( C_{\text{var}5} \) with respect to \( V_A \). For the first and the fifth operating regions,

\[
\frac{\partial C_{\text{var}1}}{\partial V_A} = \frac{\partial C_{\text{var}5}}{\partial V_A} = 0.
\]  

(4.41)

For the second and the fourth operating regions,

\[
\frac{\partial C_{\text{var}2}}{\partial V_A} = \frac{k}{\pi V_A} \sqrt{V_A^2 - (V_{CM} + V_{TH} - V_{nme} - \alpha V_H)^2},
\]  

(4.42)
and

\[
\frac{\partial C_{\text{var}3}}{\partial V_A} = -\frac{k \sqrt{V_A^2 - (V_{CM} + V_{TH} - V_{tune} + V_w (1 - \alpha))^2}}{\pi V_A}.
\] (4.43)

When the tuning voltage equals to \(V_1\) and \(V_4\), both Equations (4.42) and (4.43) evaluate to zero, as expected. For the third operating region,

\[
\frac{\partial C_{\text{var}3}}{\partial V_A} = \frac{k \left( \sqrt{V_A^2 - (V_{CM} + V_{TH} - V_{tune} - \alpha V_w)^2} - \sqrt{V_A^2 - (V_{CM} + V_{TH} - V_{tune} + V_w (1 - \alpha))^2} \right)}{\pi V_A}.
\] (4.44)

At a particular tuning voltage \(V_{\text{null}}\), Equation (4.44) evaluates to zero where,

\[
V_{\text{null}} = \frac{V_2 + V_4}{2} = V_{CM} + V_{TH} + (0.5 - \alpha) V_w.
\] (4.45)

The varactor capacitance variation with respect to the oscillating signal amplitude variation is shown in Figure 4.12. The varactor capacitance is immune to the amplitude variation in operating region one and five, since the oscillating signal experiences identical capacitance over the oscillation cycle. In operating regions two to four, one portion of the oscillating signal is within the ramp section of the \(C(V)\) curve. The variation in the oscillating amplitude affects the voltage magnitude at every time instance within the oscillation period. The changes in the voltage magnitude are converted into the capacitance variation through \(k\) in Equation (4.10). When the tuning voltage is between \(V_1\) and \(V_X\), and between \(V_Y\) and \(V_4\), \(V_{CM}\) does not enter the ramp section, and only one side of the oscillating signal enters the ramp section with \(V_{CM}\) as the center. Therefore, the capacitance variation is monotonic as the increase of the oscillating amplitude strictly leads to
the increase of the varactor capacitance, and vice versa. When the tuning voltage is between $V_X$ and $V_Y$, $V_{CM}$ enters the ramp section, and both sides of the oscillating signal stays within the ramp section. Therefore, the capacitance variation is no longer monotonic, where the oscillating amplitude variation leads to the increase of the capacitance on one side of $V_{CM}$, and decreases on the other side. Therefore, the net change in the capacitance is reduced for the same change in the oscillating amplitude and thus the magnitude of the sensitivity starts to decrease. At $V_{null}$, the capacitance increase on one side of $V_{CM}$ cancels the decrease on the other side, where the sensitivity is reduced to zero.

The simulated oscillator phase noise with respect to the tuning voltage at a small frequency offset of 100Hz is shown in Figure 4.13. The phase noise is smaller at the two extremes of the tuning range, and increases as the tuning voltage approaches $V_1$ and $V_4$. Also, a dip in the phase noise variation is observed.
when the tuning voltage is within the vicinity of \( V_{\text{null}} \). The existence of the dip has also been confirmed in references [8] and [48].

An additional advantage of the proposed capacitor divider network is the tuning voltage noise suppression. Noise coming from the control voltage, similarly as the thermal noise of the tail biasing transistor, is converted into the phase noise by the varactor. In this design, the tuning voltage noise is partially steered away from the varactor by \( C_1 \), and passed to the ground by \( C_2 \). The downside of the capacitor divider network is the reduced frequency tuning range, and three digital switches are added to compensate for the loss of the tuning range.

### 4.4 Phase Noise Reduction through the Notch Filter

The thermal noise of the tail biasing transistor at even harmonics of the oscillating frequency is also down-converted into the phase noise at the oscillating frequency, \( \omega \). In particular, the thermal noise power at \( 2\omega \) needs to be minimized.
since the conversion gain is higher at $2\omega$ compared to other even harmonics [45].

A filtering technique is proposed in Reference [17] to reduce the thermal noise power at $2\omega$ from entering the resonator, where the inductor and the capacitor together form high impedance at $2\omega$ such that the thermal noise of the tail transistor within the vicinity of $2\omega$ is isolated from the resonator.

In this work, a 2nd order notch filter is implemented as shown in Figure 4.14. The noise transfer function is given by,

$$\frac{S_{AM-out}(\omega)}{S_{AM-in}(\omega)} = \frac{s^2 L_{nf} C_{nf} + 1}{s^2 L_{nf} C_{nf} + s R_{nf} C_{nf} + 1}. \quad (4.46)$$

At both the low and high frequencies, the magnitude of the transfer function evaluates to unity. At the resonant frequency, the magnitude is zero. When the resonant frequency of the notch filter matches $2\omega$, the thermal noise power of the tail transistor within the vicinity of $2\omega$ is greatly attenuated.

With the notch filter, the inductor is no longer directly connected between the tail transistor and the resonator, where the inductor is replaced with $R_{nf}$. As a

![Figure 4.14: The proposed 2nd order notch filter in this work.](image)
result, the thermal noise associated with the series resistance of the inductor which can enter the resonator is replaced with the thermal noise associated with \( R_{nf} \). While the ease of reducing the series resistance of the inductor is limited by the required inductance to form the high impedance at \( 2\omega \), there is much more freedom in adjusting \( R_{nf} \), where \( R_{nf} \) affects only the bandwidth of the notch filter. Therefore, \( R_{nf} \) can be adjusted to a much smaller value which enlarges the bandwidth of the notch filter. The upper limit on the expanding of the bandwidth is that the lower cut-off frequency of the notch filter cannot approach the vicinity of \( \omega \) such that the signal power shall not be affected.

The series resistance of the inductor in the notch filter is connected in series with \( C_{nf} \) and \( L_{nf} \). At both the low and high frequencies, \( C_{nf} \) and \( L_{nf} \) behave as open circuit, respectively. When the thermal noise is modeled as a current source, it is connected to an open circuit at the low and high frequencies which prevents continuous current flow. At \( 2\omega \), the combined impedance of \( C_{nf} \) and \( L_{nf} \) is zero, which provides a short circuit to the power supply for the noise current.

![Figure 4.15: The simulated VCO phase noise spectrums.](image-url)
Therefore, the power spectral density of the inductor series resistance is reduced in general.

The simulated phase noise with SpectreRF in TSMC 0.18 µm technology is shown in Figure 4.15. It is evident that the phase noise at lower frequency offset has been improved by 15dB, and 5dB at higher frequency offset.

4.5 Experimental Measurement Results

Two VCOs are fabricated using TSMC 0.18µm technology, which provides 6 metal layers. The die photo is shown in Figure 4.16, and the die area is 2.2×1.8mm². Both VCOs are implemented with the top-biased complementary structure as shown in Figure 4.1(b). VCO1 consists of both the capacitor divider network and the 2nd order notch filter while VCO2 is implemented with only the capacitor divider network. The component parameters of the two VCOs are summarized in Table 4.1.

<table>
<thead>
<tr>
<th></th>
<th>Values</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{nf}$</td>
<td>10Ω</td>
<td>$W_{1/L_1}$ 800µm/1µm</td>
</tr>
<tr>
<td>$C_{nf}$</td>
<td>1.75pF</td>
<td>$W_{2-3/L_{2-3}}$ 240µm/0.18µm</td>
</tr>
<tr>
<td>$C_{1-2}$</td>
<td>5pF</td>
<td>$W_{4-5/L_{4-5}}$ 120µm/0.18µm</td>
</tr>
<tr>
<td>$C_3$</td>
<td>15pF</td>
<td>$W_{6-7/L_{6-7}}$ 800µm/3µm</td>
</tr>
<tr>
<td>$C_4$</td>
<td>2.5pF</td>
<td>$W_{8/L_8}$ 50µm/0.18µm</td>
</tr>
<tr>
<td>$R_1$</td>
<td>500Ω</td>
<td></td>
</tr>
</tbody>
</table>
The die is bond-wired in the CFP80 package, and the chip is tested with the CFP80 test fixture. Two digital switches are added to enhance the VCO tuning range, and the measured frequency tuning curve is shown in Figure 4.17. The VCO frequency is tunable from 759MHz to 912MHz, and the tuning range is 18.3%. The tank inductor is designed with the differential symmetric structure on the top metal layer with the sheet resistance of 0.036Ω/□. The thickness of the top metal layer is 0.99µm. The simulated inductance is 4.9nH with the quality factor of 5 at 900MHz. The same inductor is used for $L_{nf}$ in the notch filter. The resonant frequency of the notch filter is approximately 1.72GHz, which corresponds to 860MHz center frequency.

The measured VCO1 output spectrum is shown in Figure 4.18. The measured phase noise spectrums for the two VCOs are shown in Figure 4.19. With the addition of the notch filter, the phase noise improves by 5dB on average. At 900MHz carrier, the measured phase noise is -126.1dBc/Hz at 1MHz frequency.
offset when the VCO dissipates 4.5mW from 1.8V power supply. A performance comparison between similar designs from other groups is shown in Table 4.2. For similar Figure of Merit (FoM), this design consumes less power and provides similar tuning range as other previously proposed designs. Also, the phase noise performance is affected by the relatively low quality factor of the inductor due to the lack of availability of thicker top metal layer in the TSMC 0.18µm technology.

Figure 4.17: Measured frequency tuning characteristic of VCO1.

Figure 4.18: Measured VCO1 output spectrum.
Conclusions

A low power LC-VCO design is proposed, designed, and fabricated in TSMC 0.18 \( \mu \text{m} \) technology. The design reduces the up-conversion effect of the flicker noise due to the tail biasing transistor through a new capacitor divider varactor configuration. A notch filter is added between the biasing transistor and the LC-tank where the resonant frequency of the notch filter equals to twice the VCO oscillating frequency. As a result, the thermal noise power at twice the oscillation frequency is greatly reduced. A time-weighted approach is used to model the effective capacitance experienced by the oscillating signal over the oscillation period. Closed-form expressions of the effective capacitance are proposed, and the calculated oscillation frequency based on the modeled effective capacitance is in good agreement with the simulation results. Also, based on the modeled effective capacitance, it is mathematically verified that the flicker noise due to the tail biasing transistor is suppressed. The proposed design consumes less power compared to other designs with similar FoM.

![Figure 4.19: Measured phase noise of the two VCOs at 900MHz.](image)
### Table 4.2: Performance comparison with other designs

<table>
<thead>
<tr>
<th>Ref.</th>
<th>Frequency</th>
<th>Tuning Range</th>
<th>Phase Noise [dBc/Hz]</th>
<th>Power [mW]</th>
<th>FoM [dBc/Hz]</th>
<th>Technology</th>
</tr>
</thead>
<tbody>
<tr>
<td>[54]</td>
<td>2GHz</td>
<td>11%</td>
<td>-126 @ 600kHz</td>
<td>34.2</td>
<td>181</td>
<td>0.65µm BiCMOS</td>
</tr>
<tr>
<td>[55]</td>
<td>1.1GHz</td>
<td>28%</td>
<td>-120 @ 1MHz</td>
<td>5.4</td>
<td>181</td>
<td>0.18µm CMOS</td>
</tr>
<tr>
<td>[56]</td>
<td>1.82GHz</td>
<td>18%</td>
<td>-133 @ 1MHz</td>
<td>50</td>
<td>181</td>
<td>0.18µm CMOS</td>
</tr>
<tr>
<td>[57]</td>
<td>1.5GHz</td>
<td>14%</td>
<td>-105 @ 50kHz</td>
<td>16.2</td>
<td>182</td>
<td>0.35µm CMOS</td>
</tr>
<tr>
<td>[58]</td>
<td>5.8GHz</td>
<td>14%</td>
<td>-112 @ 1MHz</td>
<td>5</td>
<td>180</td>
<td>0.24µm CMOS</td>
</tr>
<tr>
<td>This work</td>
<td>900MHz</td>
<td>18%</td>
<td>-126.1 @ 1MHz</td>
<td>4.5</td>
<td>179</td>
<td>0.18µm CMOS</td>
</tr>
</tbody>
</table>
CHAPTER 5: GENERAL-PURPOSE HIGH-SPEED INTEGRATED LOCK-IN AMPLIFIER WITH 30Db DYNAMIC RESERVE AT 20MHz

This Chapter describes the design and implementation of a general-purpose high-speed integrated LIA. Instrumentation LIAs such as the SR830 LIA in [59] are widely used for signal detection in many general laboratory settings, where the signal frequency is less than 100kHz. The advantages of the instrumentation LIAs include setup convenience, large input and output signal dynamic range, large frequency range and huge dynamic reserve. The drawbacks include high equipment cost and huge power consumptions, where system integration with other devices is greatly limited. On-chip integrated LIAs have also been designed such as in [60][61] for a few targeted applications, where the silicon area and power consumption of the LIA chip are suitable for integration purpose.

LIAs designed for high-speed applications where the signal frequency is in the MHz range are much less common. Instrumentation LIAs offered by Stanford Research Systems Inc. [62] and Zurich Instruments Inc. [63] offer excellent performance at the expense of large size and huge power consumption. To the best knowledge, they are the only commercial available high-speed LIAs. To date, on-chip integrated high-speed LIAs are not reported in literature. In this project, a general-purpose high speed integrated LIA is reported where the frequency operating range is between 15 and 20MHz. The proposed design does not require
any off-chip components and achieves 30dB dynamic reserve with power consumption of 37mW.

Low-speed LIAs typically use the phase-sensitive detection (PSD) technique to extract the amplitude and the phase of the input signal as illustrated in Figure 5.1. The input signal is usually the sum of the signal to be detected and the noise with the spectrum spanning over a frequency range. After pre-amplification and filtering, the input signal is applied to two mixers. The reference signal with the same frequency as the input signal is also applied to the mixers. The reference signal is phase-shifted by 90° before it is applied to the second mixer. The corresponding signal spectrum is shown in Figure 5.2. The input signal with frequency $\omega$ is embedded within noise with bandwidth $B_N$. The reference signal is usually generated by an on-chip oscillator, and the signal spectrum consists of tones at $\pm\omega$, $\pm3\omega$, and so forth. The convolution of the two signals leads to the tones at DC, $\pm2\omega$, $\pm4\omega$, and so forth. The tone at DC carries the information of the input magnitude and phase, and is the signal of interest. A low-pass filter following the mixer removes the undesired harmonics and the noise. The nth

![Figure 5.1: The PSD technique used in low-speed LIA design.](image)
harmonic of the reference signal folds the high-frequency noise down to the baseband when $2n\omega < B_N$. Also, undesired tones at small frequency offset with respect to the input signal are usually hard to filter out. Therefore, low-pass filter with narrow bandwidth and faster roll-off is highly desired. For a first-order low-pass filter with cut-off frequency $f_{3\text{dB}}$, the SNR improvement due to PSD is given by,

$$SNR_{After} = \frac{2B_N}{\pi f_{3\text{dB}}} \cdot SNR_{Before}.$$  \hspace{1cm} (5.1)

$B_N$ is a modest approximation of the noise bandwidth as the total noise power is increased due to noise folding. While low pass filter with narrow bandwidth offers greater SNR improvement, the implementation usually requires extra large passive components, which is disadvantageous for on-chip integration.

PLL technique has been widely used in the communication receivers to recover signals embedded within noise. A PLL with small bandwidth averages the phase error between the input signal and the oscillator signal, where the input
random phase variation is greatly suppressed by the feedback loop. A PLL is a well fit for on-chip integration, where highly integrated frequency synthesis and data recovery circuits based on PLL are widely used in wireless and wire-line applications. Also, PLL offers a huge frequency operating range from MHz to GHz, and is well suited for high-speed applications. One disadvantage of the PLL is that it can only keep track of the phase error of the input signal while the random amplitude variation of the input signal is ignored. Therefore, PLL is only used in the phase measurement of the proposed lock-in amplifier, while the magnitude measurement is carried out with filters and time-average approach.

5.1 System Architecture

The architecture of the proposed lock-in amplifier is shown in Figure 5.3. The input sinusoidal signal to be measured is denoted as

\[ V_{SIG} = A_{SIG} (\cos \omega t + \theta_{SIG}) . \]  \hspace{1cm} (5.2)

The design is able to measure the amplitude of \( V_{SIG} \) with the Amplitude Measurement circuitry, and the relative phase difference between \( V_{SIG} \) and \( V_{REF} \) with the Phase Measurement circuitry. The measured amplitude and phase signals are denoted as \( V_{MAG} \) and \( V_{PH} \) as shown in Figure 5.3. A band-limited white noise \( V_{NOISE} \) with the bandwidth \( B_N \) is superimposed on top of the input signal through an analog adder, where the signal-to-noise ratio is denoted as \( SNR_m \). A band-pass filters with bandwidth \( f_{BPF} \) follows the analog adder, and improves \( SNR_m \) to,

\[ SNR_{After-BPF} = \frac{2B_N}{\pi f_{BPF}} SNR_m, \]  \hspace{1cm} (5.3)
where, \( f_{\text{BPF}} \) is much smaller than \( B_N \). The simulated waveforms of \( V_{\text{SIG}} \) and \( V_{\text{BPF}} \) are shown in Figure 5.4. For an arbitrary cycle \( j \), the amplitude and phase of \( V_{\text{SIG}} \) are denoted as \( A_{\text{SIG},j} \) and \( \theta_{\text{SIG},j} \), where both \( A_{\text{SIG},j} \) and \( \theta_{\text{SIG},j} \) vary from cycle to cycle due to \( V_{\text{NOISE}} \). A voltage amplifier increases the signal swing of \( V_{\text{BPF}} \) to rail-to-rail as shown in Figure 5.4. A duty cycle adjustment circuit changes the duty cycle of \( V_{\text{AMP}} \) from 50\% to 25\%. Since both \( V_{\text{AMP}} \) and \( V_{\text{CLK}} \) inherit the same \( \theta_{\text{SIG},j} \) from \( V_{\text{BPF}} \), the falling edges of \( V_{\text{CLK}} \) approximately sample the peak amplitude of \( V_{\text{BPF}} \) as shown in Figure 5.4. Multi-phase clock signals, \( \Phi \) are generated from \( V_{\text{CLK}} \), and control a switch-capacitor integrator. The integrator calculates the average value (\( V_{\text{MAG}} \)) of \( A_{\text{SIG}} \) over \( N \) cycles, where,

\[
V_{\text{MAG}} = \frac{1}{N} \sum_{j=1}^{N} A_{\text{SIG},j}.
\]  

(5.4)
$V_{AMP}$ is also used as the reference signal of a PLL with noise bandwidth $B_{PLL}$. The PLL attenuates the out-of-band random phase variation of $V_{AMP}$, and further improves $SNR_{After-BPF}$ to,

$$SNR_{After-PLL} = \frac{\pi f_{BPF}}{2B_{PLL}} SNR_{After-BPF}.$$  \hspace{1cm} (5.5)

The phase difference between $V_{PLL}$ and $V_{REF}$ are compared by a phase detector. The output of the phase detector controls a charge pump, which generates the $I_{CP}$ signal where the time-averaged magnitude of $I_{CP}$ is proportional to the phase difference between $V_{PLL}$ and $V_{REF}$. $I_{CP}$ over $N$ multiple periods are added and averaged by a current integrator, and the output signal $V_{PH}$ is given by,

$$V_{PH} = \frac{K_{PH}}{N} \sum_{j=1}^{N} (\theta_{SIG,j} - \theta_{REF}),$$  \hspace{1cm} (5.6)
where, $K_{PH}$ depends on the gain of the current integrator and will be derived later on. $N$ for both the amplitude and phase measurements can be conveniently set by the digital counters.

### 5.2 Component Descriptions of the Amplitude Measurement Circuitry

This section describes the circuit components of the amplitude measurement section of the LIA in Figure 5.3. It takes $V_{SN}$ as the input, and generates a DC signal $V_{MAG}$, where the magnitude of $V_{MAG}$ is proportional to the amplitude of $V_{SIG}$.

#### 5.2.1 Band-Pass Filter

The circuit schematic of the gm-C band-pass filter is shown in Figure 5.5 [64]. The center frequency and quality factor are given by,

$$\omega_c = \sqrt{\frac{g_{m2}g_{m3}}{C_1C_2}},$$  \hspace{1cm} (5.7)

and

![Figure 5.5: Schematic of the band-pass filter. Design parameters: $C_1=64\text{pF}$, $C_2=4\text{pF}$, $g_{m1}=g_{m2}=g_{m3} = 4g_{m4}=1.59\text{mA/V.}](image)

The feedback loop formed by trans-conductors two and three will oscillate for moderate $g_m$ values, and trans-conductor one is able to stabilize the output voltage for large $g_{m1}$ values at the cost of reduced filter quality factor. However, the effectiveness of trans-conductor one degrades as $g_{m1}$ decreases. Therefore, trans-conductor four is added to make the filter quality factor independent of $g_{m1}$. The center frequency is tuned by changing the biasing current of trans-conductor three, which effectively varies $g_m$. By setting $g_{m2}=4g_{m4}$ and $C_1=16C_2$, quality factor over 20 is achieved while the frequency tuning range is from 14-22MHz.

\[
Q = \sqrt{\frac{g_{m2}g_{m3}}{g_{m4}}} \sqrt{\frac{C_1}{C_2}}.
\] (5.8)

5.2.2 Amplifier

The voltage amplifier following the band-pass filter increases the signal swing to rail-to-rail. Since $V_{CLK}$ samples the peak value of $V_{BPF}$, it is critical that the amplifier bandwidth is high enough such that no phase shift exists between $V_{BPF}$ and $V_{AMP}$. As a result, amplifier with common source configuration is employed due to its high bandwidth and large output dynamic range.

5.2.3 Duty-Cycle Adjustment and Clock Generation

The duty cycle of $V_{CLK}$ is adjusted from 50% to 25% through the circuitry shown in Figure 5.6(a). An inverter-based voltage-controlled delay line (VCDL) as shown in Figure 5.6(b) provides half of a signal period time delay. An AND gate produces $V_{CLK}$, which is phase aligned with $V_{AMP}$.\"
$\text{VCLK}$ is converted into multi-phase clock signals $\Phi$ through the circuitry shown in Figure 5.7. As shown in Figure 5.8, the falling edge of $\text{VCLK}_\text{B}$ triggers the falling edge of $\Phi_2$, where the time delay $T_1$ is,

\[
T_1 = T_{pd,\text{Inv}1} + T_{pd,\text{NOR}2,2} + T_{pd,\text{Inv}4} + T_{pd,\text{Inv}5}.
\]  

(5.9)

Also, the falling edge of $\Phi_2$ triggers the rising edge of $\Phi_3$, and the time delay $T_2$ is given by,

\[
T_2 = T_{pd,\text{NOR}2,1} + T_{pd,\text{Inv}2} + T_{pd,\text{Inv}3}.
\]  

(5.10)

Similarly, $T_3$ is given by,

\[
T_3 = T_{pd,\text{Inv}6} + T_{pd,\text{Inv}7}.
\]  

(5.11)
\( T_4 \) equals to \( T_2 \), and \( T_5 \) is given by,

\[
T_5 = T_{pd,\text{NOR}2,2} + T_{pd,\text{INV}4} + T_{pd,\text{INV}5}.
\]  \hspace{1cm} (5.12)

The timing constraint requires that,

\[
T_1 + T_2 + T_3 < 0.25T_{CLK}.
\]  \hspace{1cm} (5.13)

At \( F_{CLK} \) equals to 20MHz, Equation (5.13) can be easily realized with CMOS sub-micron technology. \( \Phi_1 \) is delayed with respect to \( \Phi_3 \) to ensure that the charge injections due to the switches are input signal independent [65].

### 5.2.4 Programmable Counter and Switch Capacitor Integrators

The integrating step in Equation (5.4) is adjustable through the programmable count-down counter shown in Figure 5.9. The 4-bit counter consists of four S-R latch and D Flip-Flops (SR-DFFs). The count value is set through \( P_{3-0} \), and the maximum count can reach 15. When Preset is set to logic-high, the initial count of the counter is set to \( P_{3-0} \), and the end-of-count (EOC) signal is set to logic-low. The counter is triggered by setting Preset to logic-low. When the count reaches 0000, the EOC signal becomes logic-high, which forces all the inputs of the
NOR-4 gate to logic-low. Therefore, EOC is kept logic-high thereafter until Preset becomes logic-high again.

After the instance where \( V_{CLK} \) causes the counter output to be 0000, the propagation delay through DFF\(_1\), NOR4, and MUX\(_{1,2}\) cannot be longer than the period of \( V_{CLK} \) as

\[
T_{pd, DFF1} + T_{pd, MUX1} + T_{pd, MUX2} + T_{pd, NOR4} < T_{CLK}. \tag{5.14}
\]

Since \( T_{CLK} \) evaluates to 50ns, Equation (5.14) can be easily satisfied with CMOS sub-micron technology.

The schematic of the switch-capacitor integrator is shown in Figure 5.10(a). When the EOC signal is logic-low, the clock signal \( \Phi_{1,2,3} \) control the switches of the integrator. After EOC becomes logic-high, all the switches are turned off and \( V_{MAG} \) is held constant. A high-pass filter consisting of \( C_{HF} \) and \( R_{HF} \) is added to ensure that only the AC magnitude of \( V_{BPF} \) is integrated while the DC component

![Diagram of the 4-bit programmable counter](image-url)

Figure 5.9: Schematic of the 4-bit programmable counter in the magnitude measurement circuitry.
is blocked. When Preset is set to logic-high, $V_{MAG}$ is forced to be $V_{AGND}$. When Preset becomes logic-low, $V_{MAG}$ becomes

$$V_{MAG} = V_{AGND} + \frac{C_1}{C_2} \sum_{j=1}^{N} A_{4IG,j}$$

(5.15)

after N cycles.

During the integrating phase of the operation, approximately $7\tau_{OPA}$ is required for the OPAMP output to settle within 0.1% of the final value [66] where, $\tau_{OPA}$ is the time constant of the OPAMP. Since the time duration allocated to the integrating phase is $0.75T_{CLK}$, if the final value is required to settle within $0.4T_{CLK}$, $\tau_{OPA}$ should be less than 2.857ns. Since,
\[ \tau_{\text{OPA}} = \frac{1}{\beta \omega_{\text{UGB}}}, \]  

where

\[ \beta = \frac{C_2}{C_1 + C_2}, \]  

and \( \omega_{\text{UGB}} \) is the unity-gain bandwidth of the OPAMP [66]. \( \omega_{\text{UGB}} \) should be larger than 111.4MHz when \( C_1 \) equals to \( C_2 \). This is achieved through the OPAMP shown in Figure 5.10(b). \( \omega_{\text{UGB}} \) is designed to be 1.82GHz, more than a decade above the required \( \omega_{\text{UGB}} \).

5.3 Components Descriptions of the Phase Measurement Circuitry

This section describes the implementation of the phase measurement circuit of the LIA as shown in Figure 5.3. \( V_{\text{AMP}} \) is taken as the input of the PLL. The output signal \( V_{\text{PH}} \) is a DC voltage where the magnitude is proportional to the phase difference between \( V_{\text{SIG}} \) and \( V_{\text{REF}} \).

5.3.1 Phase-Locked Loop

The structure of the fractional-N phase-locked loop is shown in Figure 5.11. The reference signal of the PLL is \( V_{\text{AMP}} \) where the random phase variation of \( V_{\text{AMP}} \) due to \( V_{\text{NOISE}} \) can be filtered out by the low-pass characteristic of the PLL. The transfer function of the PLL is given by,

\[ \frac{\theta_{\text{PLL}}}{\theta_{\text{REF}}} = \frac{K_{\text{pd}} K_{\text{VCO}} F(s)}{s N + K_{\text{pd}} K_{\text{VCO}} F(s)}. \]
where, $K_{PD}$, $K_{VCO}$, $F(s)$ and $N$ represent the gain of the phase detector, the gain of the VCO, the loop filter transfer function, and the feedback division value, respectively. At low frequency offset, the random phase noise passes to the output un-attenuated. As the frequency increases beyond the PLL loop bandwidth, the PLL can no longer track the reference phase variation thus the phase noise is effectively filtered at higher frequency offset.

### 5.3.1.1 The Phase Frequency Detector and Charge Pump

The schematic of the PFD and the charge pump are shown in Figure 5.12 and Figure 5.13 respectively. The PFD is implemented based on CMOS logic, which is fully functional for the intended input frequency range. A well-known issue encountered with the PFD is the dead-zone problem, where the PFD and the charge pump cannot supply sufficient output current to the loop filter when the time difference between the reference signal and the feedback signal is smaller than the switch delay of the charge pump [8]. The reduced gain of the PFD directly leads to reduced loop bandwidth, which could make the PLL less stable.

![Figure 5.11: Schematic of the fractional-N PLL.](image)
A common approach to resolve this issue is to add extra time delay in the PFD such that the propagation delay of the PFD is longer than the switch delay of the charge pump. The apparent drawback of this approach is the addition of the extra phase error.

Figure 5.12: Schematic of the phase-frequency detector.

Figure 5.13: Schematic of the differential charge pump.
The UP and DN signal of the PFD are converted into eight control signals for the charge pump (identical circuitry for UP and DN signal) as shown in Figure 5.12(b) [67]. The control signals of the charge pump switches should not turn both branches off at any time instance in order to avoid the glitch at the drains of the biasing transistors. Therefore, the falling edge of $V_{\text{UND}}$ lags $V_{\text{UP}}$, and the rising edge of $V_{\text{UND}}$ leads $V_{\text{UP}}$ as shown in Figure 5.14. To achieve the require timing waveforms, the threshold voltages of the inverters are adjusted as shown in Figure 5.12(b), where Inverter-H has high switching threshold voltage by making the aspect ratio of the PMOS transistor much larger than that of the NMOS transistor, and vice versa. Also, cross-coupled inverters are used to ensure the phase alignment between $V_{\text{UP}}$ and $V_{\text{UN}}$. The switch sizes are made minimum to reduce the charge injection effect. A voltage follower in Figure 5.13 is added to limit the charge sharing effect [8].

### 5.3.1.2 The Loop Filter

Since the PLL can only filter phase variation at frequency offset above the PLL loop bandwidth, lower PLL loop bandwidth is highly desired in the intended
LIA application. Large passive capacitor is usually required to achieve low PLL bandwidth, and is not suitable for on-chip integration. The dual-path loop filter proposed in [68] achieves the same loop bandwidth and dynamic but with much smaller capacitance value as shown in Figure 5.15. The loop filter requires two charge pumps with output currents $I_{CP}$ and $B I_{CP}$. The first path of the loop filter consists of a current integrator, and the second path is a low-pass filter. The sum of the two paths is passed to another low-pass filter to attenuate the reference spur. The transfer function of the loop filter is given by,

$$F(s) = \frac{1}{sC_Z \left(1+s\tau_Z\right) \left(1+s\tau_P\right) \left(1+s\tau_4\right)}.$$  \hspace{1cm} (5.19)

where, $\tau_Z = B R_P C_Z$, $\tau_P = R_P C_P$ and $\tau_4 = R_4 C_4$. Therefore, for the same zero location $\tau_Z$, the required capacitance $C_Z$ can be reduced by $B$ times. The structure of the amplifier in the integrator path is a differential pair. The analog adder proposed in [69] is implemented in this design. The loop filter parameters are summarized in Table 5.1.
Table 5.1: Summary of the loop filter parameters

<table>
<thead>
<tr>
<th>Component</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{CP}$</td>
<td>26µA</td>
</tr>
<tr>
<td>$B$</td>
<td>10</td>
</tr>
<tr>
<td>$C_Z$</td>
<td>163pF</td>
</tr>
<tr>
<td>$R_P$</td>
<td>7.8kΩ</td>
</tr>
<tr>
<td>$C_P$</td>
<td>68.4pF</td>
</tr>
<tr>
<td>$R_4$</td>
<td>3.9kΩ</td>
</tr>
<tr>
<td>$C_4$</td>
<td>137pF</td>
</tr>
</tbody>
</table>

From Equation (5.19), the zero frequency is 12kHz, and the frequency of the two poles is 300kHz. The PLL loop bandwidth is given by

$$K = \frac{I_{CP} K_{VCO} R_P C_P + B C_Z}{2\pi N C_Z}, \quad (5.20)$$

which evaluates to 52.1kHz when $K_{VCO}$ equals to 78.4MHz/V. Therefore, $K\tau_Z$ and $K\tau_P$ are approximately 4.3 and 0.174, respectively.

The PLL open-loop response is simulated as shown in Figure 5.16. At low frequency, the magnitude response decreases at -40dB/dec. The zero at $\tau_Z$

![Figure 5.16: Simulated bode plot of the PLL open-loop response.](image-url)
increases the slope to -20dB/dec, and the two poles at $\tau_p$ and $\tau_4$ decrease the slope to -60dB/dec. At the crossover frequency, the phase margin is approximately 57°.

### 5.3.1.3 LC-VCO

For low power application, the top-biased complementary LC-VCO is implemented in this design as shown in Figure 5.17 due to its better phase noise performance. $L_1$ is increased several times beyond the minimum length to reduce the flicker noise power of the biasing transistor. $W_{2,3}/W_{4,5}$ is adjusted to ensure the half-cycle symmetry of the oscillating signal for better phase noise performance [70]. $L_{2,5}$ is kept at the minimum length to reduce the impact of the $M_{2,5}$ oxide capacitance on the frequency tuning range. $L_6$ is made large to extend the frequency tuning range at the expense of the degraded phase noise.
Passive capacitors $C_{1-3}$ are added to reduce the biasing transistor flicker noise up-conversion effect at the cost of the reduced frequency tuning range. $V_{B2}$ sets the biasing of the varactor, where the mid-point of the frequency tuning curve is biased at half point of the power supply.

The structure of the on-chip inductor is differential octagon implemented with single-layer top metal. The dimension of the inductor is optimized to achieve optimal quality factor over the intended operating frequency range. The performance of the LC-VCO is summarized in Table 5.2.

Table 5.2: Simulated performance summary of the LC-VCO.

<table>
<thead>
<tr>
<th>Frequency tuning range</th>
<th>885MHz-960MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCO gain</td>
<td>78.4MHz/V</td>
</tr>
<tr>
<td>Power consumption</td>
<td>3mA from 1.8V</td>
</tr>
<tr>
<td>Phase noise @ 1MHz</td>
<td>-126dBc/Hz</td>
</tr>
<tr>
<td>Phase noise @ 3MHz</td>
<td>-135dBc/Hz</td>
</tr>
<tr>
<td>Inductor Q @ 960MHz</td>
<td>5.8</td>
</tr>
</tbody>
</table>

5.3.1.4 Multi-modulus Programmable Divider

For the required input frequency range 15-20MHz and the VCO frequency tuning range, the feedback divider division ratio should reach at least 50. The multi-modulus divider proposed in [71] is implemented in this design, where the divider has 5 control bits and the maximum division ratio is 63. Since the maximum operating frequency is around 1GHz, the entire divider is implemented
with CMOS logic for lower power consumption. The divider output is taken from
the same mod 2/3 block as the input signal for best phase noise performance.

5.3.1.5 ∆Σ Modulator

An all-digital 3rd-order 3-bit MASH ∆Σ modulator is designed as shown in
Figure 5.18. The three digital phase accumulators are implemented based on full
adders and DFFs. The transfer function is given by,

\[ Y = Xz^{-3} + q_1 (1 - z^{-1})^3, \]  \hspace{1cm} (5.21)

where, \( q_1 \) is the quantization noise of the first accumulator. Since the MASH ∆Σ
modulator consists of three first order modulators, it is always stable while
providing higher order noise filtering.

\[ Y = Xz^{-3} + q_1 (1 - z^{-1})^3, \]  \hspace{1cm} (5.21)

The narrow PLL loop bandwidth leads to relatively slow settling time. To
improve the settling time, the VCO output frequency is held constant such that the
input frequency hopping is offset by the variation of the feedback fractional-
division ratio instead of the variation of the VCO frequency. For the 5MHz

![Figure 5.18: Block diagram of the MASH ∆Σ modulator.](image)
reference frequency range, 112 equal frequency increment $\Delta F$ is allocated such that $\Delta F$ is approximately 45kHz. The frequency span of each increment $\Delta F$ is

$$F_{\text{SPAN},m} = [20 - \Delta F \cdot m, \ 20 - \Delta F \cdot (m - 1)],$$

(5.22)

where, $m$ varies from 1 to 112. For the 3-bit MASH modulator, the resolution of the fractional-division ratio is $1/8$. Therefore, for each $F_{\text{SPAN},m}$, the corresponding feedback division ratio is set to

$$D_m = 45 + \frac{m}{8},$$

(5.23)

and the VCO output frequency is the product of $F_{\text{SPAN},m}$ and $D_m$. The VCO frequency with respect to the reference frequency plot is shown in Figure 5.19, where the VCO frequency varies within $\pm$15MHz over the targeted reference frequency span. For any interested input frequency between 15-20MHz, the corresponding $D_m$ is applied to the coarse and fine control in Figure 5.11. The VCO frequency is forced to be adjusted slightly to compensate for the limited resolution of the MASH modulator, and the settling time of the PLL to lock to the new reference frequency can be greatly improved.

Figure 5.19: VCO frequency variation with respect to the reference frequency due to variable feedback division ratio.
5.3.1.6 In-Lock Detector

An in-lock detector is designed to monitor if the PLL has reached the locked state. The schematic of the in-lock detector is shown in Figure 5.20, which takes the VCO control voltage $V_C$ as the input. Since the VCO output frequency span is controlled within a small range, the VCO control voltage variation is also limited. When the PLL is in the locked state, $V_C$ falls between the two boundaries set by $V_A$ and $V_B$, and the output of the two comparators are both logic-high. Six DFFs are connected in series, where the clock is controlled by $V_{PLL}$. If $V_C$ is within the range set by $V_A$ and $V_B$ for six consecutive cycles, $V_{In-lock}$ becomes logic-high to indicate that the PLL has reached the locked state.

![Figure 5.20: Schematic of the in-lock detector.](image)

When Preset signal is triggered, both $V_A$ and $V_B$ are logic-low, thus $V_{In-lock}$ is also forced to logic-low. When Preset is set to logic-low and $V_{In-lock}$ becomes logic-high, the input of the first DFF is also set to logic-high thus $V_{In-lock}$ is maintained at logic-high.
5.3.2 Programmable Counter

The schematic of the 4-bit programmable counter is shown in Figure 5.21. When $V_{\text{In-lock}}$ is at logic-low, the initial conditions of the SR-DFFs are set to $P_{3:0}$. Therefore, EOC signal is set to logic-low. When $V_{\text{In-lock}}$ is at logic-high and the counter has reached the 0000 state, EOC becomes logic-high to maintain EOC at logic-high. As a result, $V_{\text{PLLX}}$ and $V_{\text{REFX}}$ are set to logic-low to disable the downstream phase detector and charge pump.

![Schematic of the 4-bit programmable counter in the phase measurement circuitry.](image)

Figure 5.21: Schematic of the 4-bit programmable counter in the phase measurement circuitry.

5.3.3 Current Integrator

The phase difference between $V_{\text{PLL}}$ and $V_{\text{REF}}$ are measured by the phase detector and the charge pump. The charge pump current $I_{\text{CP}}$ charges the current integrator in Figure 5.22 for N period set by $P_{3:0}$ of the programmable counter. The final voltage $V_{\text{PH}}$ after N cycles is given by Equation (5.6), where,

$$K_{\text{PH}} = \frac{I_{\text{CP}}}{2\pi f_{\text{REF}} C}.$$  (5.24)
The same phase detector and charge pump in Figure 5.12 and Figure 5.13 are used in the phase measurement circuitry.

![Figure 5.22: Schematic of the current integrator.](image)

### 5.4 Measurement Results

The designed high-speed integrated LIA is fabricated in TSMC 0.18\(\mu\)m technology. The die micrograph is shown in Figure 5.23, where the chip area is 5mm\(^2\). The die is bond-wired in the CFP80 package provided by Canada Microelectronics Corporation, and the chip is tested with the CFP80 testing fixture. The reference signal and the LC-VCO output are bond-wired externally to test the performance of the PLL. When the reference of the PLL is driven by a high-purity external signal, the measured VCO phase noise is shown in Figure 5.24. The measured phase noise at 1MHz and 3MHz frequency offset are -125dBc/Hz and -131dBc/Hz at 890MHz output frequency, respectively. The PLL loop bandwidth is less than 100kHz, and the in-band phase noise is under -80dBc/Hz.
Both $V_{SIG}$ and $V_{NOISE}$ in Figure 5.3 are supplied with external power supply. At -30dB SNR and 20MHz input frequency, the measured transient response of $V_{MAG}$ is shown in Figure 5.25. During the preset phase, Preset signal is set to logic-high and $V_{MAG}$ is forced to be $V_{AGND}$ as described in Figure 5.10. During the integration phase, Preset signal is set to logic-low, and the programmable counter is enabled. Maximum 15 integrating steps increase $V_{MAG}$ to the DC level.

![Figure 5.23: Die micrograph of the fabricated high-speed LIA in TSMC 0.18µm technology.](image)

![Figure 5.24: Measured phase noise of the LC-VCO at 890MHz output frequency.](image)
voltage proportional to the amplitude of $V_{SIG}$. During the EOC phase, the switches of the switch-capacitor integrator are turned off, and $V_{MAG}$ is held constant. The variation of $V_{MAG}$ with respect to the amplitude of $V_{SIG}$ is shown in Figure 5.26. Approximately 300mV variation of $V_{MAG}$ corresponds to 600mV variation of $V_{SIG}$ amplitude, which translates to 0.5V/V sensitivity.

Figure 5.25: Measured transient waveforms at the output of the magnitude measurement circuitry. Top: 100mV input signal amplitude. Bottom: 700mV input signal amplitude. Yellow: $V_{MAG}$. Blue: Preset signal.
Also, the measured transient response of $V_{PH}$ at 20MHz input frequency is shown in Figure 5.27. The measured $V_{PH}$ with respect to the phase difference between $V_{SIG}$ and $V_{REF}$ is shown in Figure 5.28, where $V_{PH}$ varies approximately 182mV for 60 degrees of phase difference. The sensitivity of the phase measurement circuitry is 3mV/degree at -30dB SNR.

The performance of the high-speed LIA is compared with the existing designs (including integrated low-speed LIAs and commercial large-sized high-speed LIAs) in Table 5.3. Compared to the low-speed integrated LIAs from [21][22][72], the proposed LIA provides a decent output dynamic range while consuming relatively equivalent amount of power. The commercial large-sized high-speed instrumentation LIA in [62] well exceeds the dynamic reserve and output dynamic range performance compared to the proposed design. On the other hand, the proposed design offers an on-chip integrated approach to realize the magnitude and phase detection capability at much lower power consumption.

![Figure 5.26: Measured DC output voltage with respect to the input signal amplitude.](image)
Figure 5.27: Measured transient waveforms at the output of the phase measurement circuitry. Top: 30° phase difference. Bottom: 90° phase difference. Yellow: $V_{PH}$. Blue: Preset signal.

Figure 5.28: Measured DC output voltage with respect to the phase difference between the input signal and the reference signal.
Table 5.3: Performance comparison with existing designs.

<table>
<thead>
<tr>
<th>Frequency</th>
<th>Technology</th>
<th>Dynamic reserve</th>
<th>Power consumption</th>
<th>Output Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>[21]</td>
<td>20kHz</td>
<td>CMOS 0.7µm</td>
<td>-</td>
<td>25mW, 0.3V-0.55V</td>
</tr>
<tr>
<td>[22]</td>
<td>30kHz</td>
<td>CMOS 0.35µm</td>
<td>40dB</td>
<td>110mW, -0.2V-0.4V</td>
</tr>
<tr>
<td>[72]</td>
<td>1kHz</td>
<td>CMOS 0.18µm</td>
<td>-</td>
<td>2mW, 1.04V-1.18V</td>
</tr>
<tr>
<td>[62]</td>
<td>25kHz-200MHz</td>
<td>-</td>
<td>80dB</td>
<td>70W, 100mV-1V</td>
</tr>
<tr>
<td>This Work</td>
<td>15-20MHz</td>
<td>CMOS 0.18µm</td>
<td>30dB</td>
<td>37mW, 0.54V-0.85V</td>
</tr>
</tbody>
</table>

5.5 Conclusion

In this design, a general-purpose high-speed integrated LIA is designed. The designed LIA consists of the magnitude and phase measurement circuitry components to extract the input signal magnitude and phase where the SNR can be as worse as -30dB. The magnitude measurement circuitry relies on the bandpass filter and a current integrator to generate the $V_{MAG}$ signal where $V_{MAG}$ is directly proportional to the input signal amplitude. The phase measurement circuitry uses a low-bandwidth PLL and current integrator to generate the $V_{PH}$ where $V_{PH}$ is directly proportional to the phase difference between the input signal and the reference signal. The designed LIA is fully integrated and requires no off-chip components. It consumes 37mW of power while providing reasonable output dynamic range, and magnitude and phase measurement sensitivity.
CHAPTER 6: FUTURE WORK

The low-speed LIA for fluorescence signal detection proposed in Chapter 2 targets on signal magnitude extraction of the input optical signal. Phase extraction between the input signal and the reference signal is also desired, where phase sensitive detection technique can be applied.

The proposed time-average approach to model the LC-VCO oscillating frequency characteristic in Chapter 4 has assumed that the oscillating signal is a perfect sine wave, where only the fundamental tone exists. In reality, even-order harmonics of the oscillating signal also exist due to the variable capacitance of the varactor. To improve the accuracy of the proposed model, the impact of the even-order harmonics on the oscillating frequency also needs to be modeled and analyzed. The significance of improving the oscillating frequency model is to gain more practical insight on VCO phase noise improvement. The harmonics induced from different noise sources contribute to the VCO phase noise, and no closed-form expressions of the harmonics as functions of VCO design parameters exist in the literature yet. Therefore, the designers mainly rely on experience and general rule of thumbs to obtain desired VCO phase noise performance. If precise mathematical expressions of output signal harmonics are developed, noise sources and their respective contributions are transparent, and phase noise optimization can be carried out with much less effort and great precision.
The high-speed integrated LIA proposed in chapter 5 has been designed and tested for electrical signals, where the input signals are generated from instrumentation power supply. To apply the designed LIA in more application-specific fields, the interface between the LIA chip and the detecting sensor is required. Since the minimum detectable voltage of the LIA chip is in the mV range, pre-filtering and amplification of the sensor signal are mandatory. Also, the input detectable range is from 100mV to 700mV. This can be greatly improved compared to the input detectable range of the commercial instrumentation LIA, which falls within the microvolt range. To accommodate such small input voltage, ultra low-noise and high gain amplifiers are required to improve the signal power. Also, the LIA dynamic reserve has large room for improvement, where better performance of electronic components are required. In particular, filters with much higher quality factors are mandatory.
REFERENCES


[63] HF2LI lock-in amplifier, Zurich Instruments.