An Anti-Aliasing Filter based on
Continuous-Time Delta-Sigma Modulation

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October 2009

A thesis submitted to McGill University in partial fulfilment of the requirement of
the degree of Master of Engineering

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An anti-aliasing filter that incorporates a sampler is proposed. Its architecture is inspired by the anti-aliasing filtering property of continuous-time (CT) $\Delta\Sigma$ modulators. However, contrary to CT $\Delta\Sigma$ modulators, the proposed sampling anti-aliasing filter is not sensitive to clock jitter. Furthermore, its key characteristics include: 1) high suppression of aliases - for example, compared to a Butterworth filter of the same order - owing to its notches at multiples of the sampling frequency; 2) high-pass shaping of sampling errors, similar to the shaping of quantization noise in $\Delta\Sigma$ modulators; and 3) its alias suppression is preserved over a broad range of sampling frequencies, thereby enabling its use as a general-purpose intellectual property (IP) block. Thus, the proposed sampling anti-aliasing filter is particularly attractive at the input of noise-shaping analog-to-digital converters (ADCs), such as discrete-time (DT) $\Delta\Sigma$ ADCs. Its performance advantages are derived theoretically and confirmed through simulations.
Un Filtre Anticrénelage baseé sur Temps Continu Delta-Sigma Modulation

Pavel Peev

RÉSUMÉ

Un filtre anticrénelage qui incorpore un échantillonneur est proposé ci-après. Son architecture s’inspire des propriétés d’anticrénelage des modulateurs ΔΣ en temps continu (TS). Néanmoins, contrairement aux modulateurs ΔΣ TC, le filtre proposé n’est pas victime de la sensibilité au bruit d’horloge. De plus, ce filtre anticrénelage possède entre autres les qualités suivantes: 1) Réduction élevée des créneaux non désirés - en comparaison par exemple aux créneaux d’un filter Butterworth du même ordre - ceci grâce à la présence de points rejet dans le réponse du filtre aux multiples de la fréquence d’échantillonnage; 2) Transformation passe-haut des erreurs d’échantillonnage, de façon similaire à la transformation du bruit de quantification dans les modulateurs ΔΣ; 3) Préservation de la suppression des créneaux a travers une bande large de fréquences d’échantillonnage; ce qui en permet l’usage banalisé sous forme de block de propriété intellectuelle (PI). Ainsi, le filtre d’échantillonnage anticrénelage proposé ci-après est particulièrement adéquat à l’entrée de la transformation de bruit d’un convertisseur analogue-numérique (CAN) comme les CAN a temps discrets. La performance de ce filtre est dérivée de manière théorique et confirmée par des simulations.
I would like to express my gratitude to my supervisor, Prof. A. A. Hamoui. He has given me the opportunity to gain experience in crucial aspects of research from forming ideas to writing papers. Furthermore, he has allowed me to gain experience as a Teaching Assistant, a job I enjoyed immensely.

I would like to thank all of my colleagues, past and present, at the Integrated Circuits and Systems Group. Their willingness to discuss, help, and especially their companionship, made my work much more enjoyable. Specifically, I would like to thank Mohammad Alghamdi, Furrookh Ali, Phil Chopp, Mostafa Haroun, Aniroodh Mehta, Mohamed Shaheen, Mohamed Sukhon, and Mohammad Taherzadeh-Sani.

Furthermore, I would like to thank Bart de Vuyst and Professor Pieter Rombouts for their input and help in publishing the conference paper on which parts of Chapter 2 are based upon.

Finally, I would like to thank those closest to me: my family, my beautiful and very supportive girlfriend Martina Doytchinova, and my good friends.
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Chapter 1

Introduction

1.1 Overview

When a continuous-time signal is sampled at a frequency $f_S$, signal components beyond $f_S/2$ alias into the Nyquist band $[0, f_S/2]$. To avoid aliasing distortion, the analog signal at the input of an analog-to-digital converter (ADC) is first bandlimited to the Nyquist band using an analog low-pass filter (i.e., an anti-aliasing filter), and then sampled at $f_S$. In a ΔΣ ADC, the requirements on the anti-aliasing filter are relaxed, as the signal band is smaller than the Nyquist band multiplied by the oversampling ratio.

Continuous-time (CT) ΔΣ modulators have recently gained popularity, owing to their potential for low-power high-speed operation [Breems, JSSC07][Mitteregger, JSSC06], shaping of sampling errors, and implicit anti-aliasing filtering [Candy, ITC85][Keller, ISCAS07][Shoaei, TCASII97]. Discrete-time (DT) ΔΣ modulators are still preferred in many applications, as they do not require tuning circuits or suffer from clock-jitter sensitivity [Chopp, ISCAS07][Reddy, TCASI07], compared to CT ΔΣ modulators. Furthermore, the noise-shaping characteristics of DT ΔΣ modulators scale with $f_S$, thereby enabling their use as general purpose ADCs. However, one drawback of DT ΔΣ modulators is that they require an explicit anti-aliasing filter, as the analog signal is sampled at the modulator input.

One solution is to use mixed CT/DT ΔΣ modulators, which combine the advantages of CT and DT ΔΣ modulators [Nguyen, JSSC05]. However, among other issues, they still suffer from
clock jitter, as the quantized DT feedback pulse is subtracted from a CT input signal [Morrow, ISSCC05]. Also, many mixed CT/DT ΔΣ modulators are designed with one CT stage; thus the anti-aliasing protection is minimal [Nguyen, JSSC05][Putter, ISSCC07][Morrow, ISSCC05]

Another solution is to use a CT filter to perform the anti-aliasing operation, followed by the DT ΔΣ ADC. Possible CT filters include Elliptic, inverse Chebyshev, and Butterworth filters. The advantage of Elliptic and inverse Chebyshev filters is that they have notches that can be placed at multiples of $f_S$ thus blocking interferers that would alias inband. The drawback of such filters is that they have a finite number of notches, and tuning circuitry is necessary in order to place the notches accurately. Butterworth filters do not have notches and require tuning circuitry to make the filter programmable as in [Chamla, JSSC07]. Furthermore, none of these filters incorporate a sampler, thus the sampling errors in the first stage of the ADC would limit the ADC’s overall resolution.

An integration sampler, such as the one proposed in [Mirzaei, TCASI08], offers notches at multiples of $f_S$ as well as a sampler with good noise performance. However, the ideal behaviour is limited to a first-order filter, and a second-order filter suffers from nonidealities including notches that move away from the desired frequency, as shown in [Mirzaei, CICC05].

This paper proposes a novel anti-aliasing filter that incorporates a sampler. The filter architecture is inspired by the anti-aliasing filtering property of a CT ΔΣ modulator. However, contrary to CT ΔΣ modulators, the proposed sampling anti-aliasing filter does not suffer from clock-jitter sensitivity. Furthermore, its key features include: 1) high suppression of aliases - for example, compared to a Butterworth filter of the same order, owing to the notches at multiples of $f_S$ in its magnitude response; 2) high-pass shaping of sampling errors (similar to the shaping of quantization noise in a ΔΣ modulator); and 3) its alias suppression is preserved over a broad range of sampling frequencies, thereby enabling its use as a general-purpose intellectual property (IP) block. Thus, the proposed filter is particularly attractive at the input of DT ΔΣ modulators.
Table 1.1 Literature review of recent anti-aliasing or channel selection filters with bandwidths in the range of several MHz.

<table>
<thead>
<tr>
<th>Publication</th>
<th>Application</th>
<th>Type</th>
<th>Order</th>
<th>BW (MHz)</th>
<th>DR (dB)</th>
<th>Supply (V)</th>
<th>Technology</th>
<th>Power (mW)</th>
<th>FOM</th>
</tr>
</thead>
<tbody>
<tr>
<td>[D'Amico, JSSC06]</td>
<td>UMTS/WLAN</td>
<td>active-Gm-RC Bessel</td>
<td>4</td>
<td>1.45-3.6, 5.87-19.44</td>
<td>81</td>
<td>1.2</td>
<td>0.13um CMOS</td>
<td>3.4 (2.11MHz)</td>
<td>96.6</td>
</tr>
<tr>
<td>[Amir-Aslanzadeh, JSSC09]</td>
<td>SDR (ADSL UMTS, IEEE 802.1n)</td>
<td>active-RC Chebyshev/Inverse Chebyshev</td>
<td>1/3/5</td>
<td>1-20</td>
<td>71.4 (1-5MHz)</td>
<td>1</td>
<td>0.13um CMOS</td>
<td>3-7.5 (5th at 1MHz)</td>
<td>1312</td>
</tr>
<tr>
<td>[Chamla, JSSC07]</td>
<td>SDR (GSM to WCDMA)</td>
<td>Gm-C Butterworth</td>
<td>3/5</td>
<td>0.1-2.75</td>
<td>67</td>
<td>1.2</td>
<td>0.13um CMOS</td>
<td>1.7-2.8 (3rd) 1.8-3.3 (5th)</td>
<td>2573</td>
</tr>
<tr>
<td>[Mirzaei, CICC05]</td>
<td>SDR (GSM, WCDMA, WLAN)</td>
<td>gm-C notch</td>
<td>2</td>
<td>0.1-16</td>
<td>74 (100kHz)</td>
<td>1.2</td>
<td>0.13um CMOS</td>
<td>7.2</td>
<td>43000</td>
</tr>
<tr>
<td>[Vasilopoulos, JSSC06]</td>
<td>UMTS/CDMA</td>
<td>active-RC Chebyshev/Elliptic</td>
<td>3/5</td>
<td>5 or 10</td>
<td>73 (5MHz)</td>
<td>1</td>
<td>0.12um CMOS</td>
<td>6.1</td>
<td>369</td>
</tr>
<tr>
<td>[Lo, TCASI07]</td>
<td>channel selection</td>
<td>Gm-C Elliptic</td>
<td>5</td>
<td>(0.00025-1)</td>
<td>48</td>
<td>1.8</td>
<td>0.18um CMOS</td>
<td>0.8</td>
<td>76529 (1MHz)</td>
</tr>
</tbody>
</table>
1.2 Literature Review

In the literature, anti-aliasing filters are sometimes referred to as channel selection filters [Chamla, JSSC07], since both types of filters are responsible for filtering adjacent channels. Furthermore, many of these filters are designed to be programmable both in terms of order and channel bandwidth [Chamla, JSSC07] [Amir-Aslanzadeh, JSSC09] [Vasilopoulos, JSSC06]. In this thesis, the anti-aliasing filter was designed for a bandwidth of 2MHz to be used in applications such as UMTS. Therefore, in order to fairly compare the proposed anti-aliasing filter to other CT channel-selection/anti-aliasing filters, filters with comparable bandwidths and low supply voltages were sought.

Table 1.1 lists recent CT filter publications with bandwidths that include several MHz. The figure of merit (FOM) used to compare the filters is [D’Amico, JSSC06]:

\[
FOM = \frac{P}{8kTf_{3dB}^3N \cdot DR}
\]  

(1.1)

where \( P \) is the power, \( k \) is the Boltzmann constant, \( T \) is the temperature (300K is used in Table 1.1), \( f_{3dB} \) is the baseband bandwidth, \( N \) is the order, and \( DR \) is the dynamic range. Since all the filters are programmable, some papers simply give the range of values for their specifications. Therefore, if possible, the FOM was calculated for the values given that are closest to the targeted 2MHz bandwidth in this thesis. Otherwise, it was assumed that in the specification ranges, a higher filter order and higher bandwidth results in higher power. Furthermore, for filters that could be programmed at different orders, the FOM reported is the lowest one calculated. Observe that the DR in Table 1.1 is specified for a bandwidth if it was explicitly specified in the paper. Table 1.1 includes a variety of filter implementations such as an integrated sampler in [Mirzaei, CICC05], which is the only filter that incorporates notches and a sampler.

Finally, although the anti-aliasing filter proposed in this thesis can be compared to other channel selection/anti-aliasing CT filters, such as in Table 1.1, it should be realized that our filter possesses advantages that are not quantified in the FOM, such as notches around the sampling
frequency and shaping of sampling errors. These advantages, and others, are discussed in detail throughout the thesis.

1.3 Thesis Outline

The remainder of the thesis is organized as follows:

Chapter 2: Proposed Anti-Aliasing Filter Based on Continuous-Time $\Delta\Sigma$ Modulation

This chapter explains the fundamental ideas behind the proposed anti-aliasing filter. It derives the performance of the filter theoretically, basing it on the STF analysis of CT $\Delta\Sigma$ modulators. Also, the proposed filter is compared to the common Butterworth filter in terms of performance. Furthermore, the implementation of the proposed filter, combined with the first stage of the DT $\Delta\Sigma$, is discussed including the effects of nonidealities.

Chapter 3: Behavioral Simulations of the Proposed Anti-Aliasing Filter

This chapter discusses the nonidealities associated with the proposed filter. It includes modeling and simulation results for thermal noise, clock-jitter, nonlinear gain, and signal swing. Furthermore, the integrators and S/H circuit are modeled and the impact of the nonidealities on the design are analyzed.

Chapter 4: Circuit-Level Design and Simulation of the Proposed Anti-Aliasing Filter

This chapter discusses the circuit-level design of the various blocks of the proposed filter. The opamp design specifications, measured specifications, and component values are given. The clock generator and the generated waveforms are also shown. Finally, final transistor level simulation results are shown and compared to the ideal and nonideal behavioral models.
Chapter 5: Conclusions

This chapter summarizes the thesis and its contributions. It also offers ideas for future work that can be explored based on the work in this thesis.
Chapter 2

Proposed Anti-Aliasing Filter Based on Continuous-Time $\Delta\Sigma$ Modulation

2.1 Anti-Alias Filtering in CT $\Delta\Sigma$ Modulators

The implicit anti-aliasing property of CT $\Delta\Sigma$ modulators was first reported in [Candy, ITC85], and has since been studied extensively for various modulator architectures [Keller, ISCAS07],[Shoaei, TCASI97]. This section derives the implicit anti-aliasing property of CT $\Delta\Sigma$ modulators. The equations derived here will then be utilized in Section 2.2 to design the proposed anti-aliasing filter. Consider the linear model of a CT $\Delta\Sigma$ modulator in Fig. 2.1a, consisting of a cascade of CT integrators with distributed feedback. This model can be redrawn as depicted in Fig. 2.1b, with a loop filter $H(s)$ and an input filter $G(s)$:

\[
G(s) = \frac{1}{(sT_s)^N} \prod_{i=1}^{N} a_i
\]  

(2.1)

\[
H(s) = \frac{a_N}{sT_s} + \frac{a_Na_{N-1}}{(sT_s)^2} + \ldots + \frac{1}{(sT_s)^N} \prod_{i=1}^{N} a_i
\]  

(2.2)

Define an equivalent DT loop filter:

\[
H_{eq}(z) \equiv \text{IIT}\{H(s)H_{DAC}(s)\} = Z\left\{L^{-1}\{H(s)H_{DAC}(s)\} \big|_{t = nT_s}\right\}
\]  

(2.3)
where \( \text{IIIT} \{.\} \) denotes the impulse invariant transform, while \( Z \{.\} \) and \( L \{.\} \) denote the Z transform and Laplace transform, respectively. Here, \( T_S = 1/f_S \) is the clock sampling period. The output of the CT \( \Delta \Sigma \) modulator (Fig. 2.1b) can then be expressed as:

\[
Y(z) = \left[ \frac{G(s)}{1 + H_{eq}(e^{sT_s})} X(s) \right] + \frac{1}{1 + H_{eq}(z)} Q(z)
\]  

(2.4)

where * denotes the sampling operation, as in [Maeyer, TCASI07]. Thus, the noise transfer function (from \( Q \) to \( Y \)) is given by:

\[
NTF(z) \equiv \left. \frac{Y(z)}{Q(z)} \right|_{X(s) = 0} = \frac{1}{1 + H_{eq}(z)}
\]

(2.5)
Furthermore, the signal-transfer function (STF) before the sampler is given by:

\[
STF(s) \equiv \frac{Y(e^{sT_s})}{X(s)} \bigg|_{Q(z) = 0} = \frac{G(s)}{1 + H_{eq}(e^{sT_s})} = G(s)NTF(e^{sT_s})
\]  \hspace{1cm} (2.6)

Accordingly, to represent the CT ΔΣ modulator in Fig. 1b, the open-loop equivalent model in Fig. 2.1c can be utilized.

To illustrate how the STF in equation (2.6) results in anti-aliasing filtering, consider for example a 2\textsuperscript{nd}-order CT ΔΣ modulator (Fig. 2.1a, \(N = 2\)) with its digital-to-analog converter (DAC) effectively consisting of a zero-order hold:

\[
H_{DAC}(s) = \frac{1 - e^{-sT_s}}{s}
\]  \hspace{1cm} (2.7)

Figure 2.2 plots the magnitude response of the corresponding \(STF(s)\) in (2.6), along with its components \(G(s)\) and \(NTF(e^{sT_s})\). Observe that the STF has notches at multiples of the sampling frequency \(f_S\).

Signals that will alias into the input-signal band are found in the frequency ranges defined by \(kf_S \pm f_{BW}\), where \(f_{BW}\) is the input-signal band edge and \(k\) is an integer. The oversampling ratio is defined as:

\[
OSR \equiv \frac{f_S}{2f_{BW}}
\]  \hspace{1cm} (2.8)

Since \(OSR \gg 1\), the signals that will alias into the input-signal band are the signals close to the STF notches at multiples of \(f_S\). Therefore, these signals are suppressed, before being aliased by the sampling operation. Furthermore, as the OSR increases, these signals occur closer to the STF notches and, hence, the amount of alias suppression is higher.
2.2 Proposed Anti-Aliasing Filter

2.2.1 Filter Architecture

To design a circuit that combines anti-aliasing filtering and sampling, this paper proposes a CT ΔΣ modulator without a quantizer, as depicted in Fig. 2.3a. It is implemented using a cascade of CT integrators with distributed feedback (rather than feedforward), as this results in an equivalent forward filter $G(s)$ with only poles and, hence, maximizes the achievable anti-aliasing suppression. A zero-order hold (ZOH)

$$ZOH(s) = \frac{1 - e^{-sT_s}}{s}$$

is used as a pulse shaper to form the DT-CT interface.

The proposed anti-aliasing filter (Fig. 2.3a) does not suffer from clock-jitter sensitivity (compared to CT ΔΣ modulators), since it has no quantizer. Furthermore, since the sampler is

![Figure 2.2](image-url)
incorporated inside the loop, sampling errors are high-pass shaped (similar to the shaping of quantization noise in a ΔΣ modulator). However, the trade-off is that a sample-and-hold circuit is needed to implement the sampler. Accordingly, the proposed anti-aliasing filter is particularly attractive at the input of noise-shaping ADCs, such as DT ΔΣ modulators.

2.2.2 Open-Loop Equivalent Representation

Since the derivation of the anti-aliasing property of CT ΔΣ modulators in Section 2.1 involved setting \( Q(z) = 0 \), this analysis is applicable to the proposed anti-aliasing filter in Fig. 2.3a. Therefore, based on (2.6), the transfer function from the input \( X(s) \) to the output before the sampler \( Y(e^{st}) \) (i.e. the STF) for the proposed anti-aliasing filter (Fig. 2.3b) can be expressed as:

\[
F_{AA}(s) = \frac{Y(e^{st})}{X(s)} = G(s)NTF(e^{st})
\]  

(2.10)

where, based on (2.3) and (2.5):

\[
H_{eq}(z) = IIT\{H(s)ZOH(s)\}
\]

\[
NTF(z) = \frac{1}{1 + H_{eq}(z)}
\]  

(2.12)

Furthermore, owing to the cascade of integrators (Fig. 2.3a), the equivalent discrete-time filter \( H_{eq}(z) \) is low pass, with all of its poles at \( z = 1 \) (dc) and with the location of its zeros determined by integrator coefficients \( a_i \). Therefore, the corresponding NTF can be expressed as:

\[
NTF(z) = \frac{(z-1)^N}{\prod_{p=1}^{N} (z-z_p)}
\]  

(2.13)

where the location of the poles \( z_p \) depends on the coefficients \( a_i \). Thus, \( NTF(z) \) has a high-pass characteristic with notches at multiples of \( f_S \). Hence, in the proposed anti-aliasing filter (Fig. 2.3a), sampling errors \( N_S(z) \) are high-pass shaped, similar to the shaping of quantization noise in ΔΣ modulators (Fig. 2.1a). Thus, the open-loop equivalent model in Fig. 2.3b can be used to represent the proposed sampling anti-aliasing filter. Note that as \( f_S \) increases, the noise due to sampling
errors may increase because of imperfections in the sampling process. However, due to oversampling and shaping by the NTF, the effect of the errors will be minimized in the inband frequencies.

2.3 Circuit-Implementation of the Proposed Anti-Aliasing Filter

2.3.1 Implementation of the Sample-and-Hold Circuit

The sampling switch and ZOH in Fig. 2.3a can implemented together to form a sample-and-hold (S/H) circuit. One possible S/H circuit, shown in Fig. 2.4, is a simplified version of the circuit in [Gatti, JSSC92]. Observe that $A_1$ and $A_2$ are the first and second gain stages of a two-stage amplifier, where $C_C$ is the Miller compensation capacitor. During $\phi_1$, the sampling capacitor $C_S$ is charged by the input. When $\phi_1$ opens, the input is sampled onto $C_S$. Then $\phi_2$ is closed, connecting the opamp in feedback, and updating the output voltage $v_{out}$. Observe that when $\phi_2$ is
2.3.2 Combining the Sample-and-Hold with a DT Integrator

The proposed anti-aliasing filter in Fig. 2.3a is in front of a DT ΔΣ as show in in Fig. 2.5. Furthermore, the sampling switches of the S/H must be shared with the first stage of the DT ΔΣ (a DT integrator) in order for the sampling errors to be shaped. A possible circuit implementation, using the S/H in Fig. 2.4, is shown in Fig. 2.7. Observe that switches $S_1$-$S_2$, and the sampling
Chapter 2: Proposed Anti-Aliasing Filter Based on Continuous-Time ΔΣ Modulation

The new circuit has three distinct phases: 1) sampling of the input onto $C_S$ when $S_1$ and $S_2$ are closed 2) updating the output of the S/H circuit when $S_6$ and $S_7$ are closed; and 3) transferring the charge from $C_S$ to $C_F$ (integrating) when $S_3$ and $S_4$ are closed. These three phases must occur within one sampling period, and the operation of the DT integrator should be minimally affected.

A delaying and non-delaying DT integrator have the transfer function $I_1(z) = z^{-1}/(1 - z^{-1})$ and $I_1(z) = 1/(1 - z^{-1})$, respectively, and are normally implemented as shown in Fig. 2.6 (with the non-delaying clocks in brackets). However, with reference to Fig. 2.7, due to the sharing of capacitor $C_S$, are shared by the S/H and DT integrator, hence shaping of sampling errors from those switches is achieved.
switches $S_1$-$S_2$ and the sampling capacitor $C_S$, as well the addition of switches $S_6$ and $S_7$ in the S/H, the implementation of the integrator is modified as shown in Fig. 2.8 (here $v_{in}$ is the output of the last integrator in the proposed anti-aliasing filter). In the case of the delaying integrator, the circuit operates as follows: During $\phi_{1A}$ (assume for now that $\phi_{1A}$ and $\phi_{1Ad}$ are coincident), $C_S$ is charged by the CT filter. When $\phi_{1A}$ opens, the input is sampled onto $C_S$. Then $\phi_{1B}$ is closed, connecting the S/H op-amp in feedback and updating the output voltage, $v_f$, of the S/H circuit, where it is held by $C_C$. Next, $\phi_{1B}$ opens and $\phi_2$ (assume that $\phi_2$ and $\phi_{2A}$ are coincident) is closed, hence, the charge on $C_S$ is transferred and integrated by the first stage of the DT $\Delta\Sigma$. Again, observe that while $\phi_{1B}$ is open, the sampled voltage continues to be held on $C_C$, making the S/H circuits behave like a NRZ DAC.

The clock waveforms for both the delaying and non-delaying integrator are shown in Fig. 2.9. Clocks $\phi_{1A}$ and $\phi_{1B}$ occur while $\phi_1$ is high, allowing clock $\phi_2$ to remain unchanged, thus keeping the charge transfer phase of the DT integrator unchanged from the normal integrator. Hence, the settling time and power consumption of the DT integrator are not affected by the modified timing of the switches.

Figure 2.8 The modified delaying (non-delaying) integrator with the S/H circuit and clock phases.
2.3.3 The Effect of the Nonideal Sample-and-Hold Behavior

**Effect on the DT Integrator**

Since the charge transfer phase of the DT integrator is vital to minimizing power and settling time, the loading effect of the S/H circuit is important. Figure 2.10 shows the charge transfer phase of a normal integrator, in addition to the first stage $A_1$ of the two-stage opamp in the S/H circuit ($\phi_2$ is high in Fig. 2.7). In a normal integrator (Fig. 2.6), the input capacitance is given by

\[ C_{in} = C_p + C_{gs,DT} \]  

(2.14)
where \( C_p \) is the parasitic capacitance of \( C_S \) and \( C_F \), and \( C_{gs,DT} \) is the gate to source capacitance of the DT integrator’s opamp. However, in the modified integrator, the input capacitance is given by

\[
C_{in} = C_p + C_{gs,DT} + C_{gs,SH}
\]  
(2.15)

where \( C_{gs,SH} \) is the gate to source capacitance of the first stage \( A_1 \) of the S/H opamp. Therefore, with respect to a normal integrator having the same \( C_S \), \( C_{in} \) increases due to the additional parasitic capacitance introduced by the S/H circuit.

The effect of \( C_{in} \) during the charge transfer phase has been analyzed in detail in [Hamoui 04]. Briefly, an increase in \( C_{in} \), due to \( C_{gs,SH} \), results in a decreased feedback factor and ultimately increased settling time. Therefore, the opamp of the DT integrator would need to have its power consumption increased in order to keep the settling-time similar to a regular integrator. However, in a regular integrator the thermal noise \( (kT/C_S) \) of all the switches (S1-S4 in Fig 2.7) adds together and ultimately set the size of \( C_S \). In the modified integrator, noise from switches S1 and S2 (in Fig 2.7) is shaped, allowing for the size of \( C_S \) to be substantially reduced, and thus reducing the associated parasitic capacitance, \( C_p \). Consequently, the reduction in \( C_p \) may be large enough to offset the addition of \( C_{gs,SH} \) and to keep the power consumption of the modified DT integrator similar to the normal DT integrator. In fact, if to begin with \( C_S \) was very large (resulting in a large \( C_p \)) in the normal integrator, then the power requirement on the DT integrator may even be reduced in the modified version due to the potential to substantially decrease \( C_S \) (resulting in a smaller \( C_p \)).

**Effect on the Anti-Aliasing Filter**

The opamp of the S/H takes a finite time to settle due to to its finite gain-bandwidth. Furthermore the final settling value has an error of \( 1/(1 + A) \) due to the finite gain of the opamp. Hence, the feedback pulse is less than ideal as illustrated in Fig. 2.11. However, because of oversampling and the absence of a quantizer, the change in voltage levels between samples will be small resulting in relaxed slew rate conditions, and ideally no slewing. Therefore, the opamp will
always exhibit the same settling behaviour (apart from jitter and nonlinear gain in the opamp which are analyzed in Chapter 3). This type of error in the feedback pulse shape is easily compensated for by slightly modifying the feedback coefficients (in the same way that the feedback coefficients would be modified for a return-to-zero (RZ) pulse shape). Therefore, the specifications of the opamp in the S/H are relaxed allowing for a low-power solution. However, observe that the nonlinearity of the S/H, due to the nonlinear gain of the S/H opamp, is not shaped and thus it sets the linearity of the whole system.

2.4 Performance Analysis of the Proposed Anti-Aliasing Filter

2.4.1 Minimum Alias Suppression

The signals that will alias into the input-signal band are found in the frequency ranges $kf_S \pm f_{BW}$ $(k = 1, 2, \ldots)$. Therefore, since the anti-aliasing filter is lowpass, the signals at the band edge of the first image $f = f_S - f_{BW}$ receive the least suppression. Hence, the inverse magnitude response of the anti-aliasing filter at $f = f_S - f_{BW} = f_S(1 - 1/(2OSR))$ corresponds to the worst-case suppression of aliases by the anti-aliasing filter. This is referred to as the minimum alias suppression.
Accordingly, substituting (2.1) and (2.13) into (2.10), the minimum alias suppression of the proposed anti-aliasing filter can be expressed as:

\[
MS_{AA} \equiv \frac{1}{|F_{AA}(j2\pi f)|} \bigg|_{f=f_{S}-f_{BW}} \\
= \frac{|j2\pi f T_s|^N}{\prod_{i=1}^{N} a_i} \left| \prod_{p=1}^{N} \left| \frac{e^{j2\pi f T_s} - z_p}{e^{j2\pi f T_s} - 1} \right|^N \right|_{f=f_{S}-f_{BW}}
\]  

(2.16)

To simplify (2.16), observe that:

1) For \( OSR >> 1 \):

\[
e^{j2\pi (f_{S}-f_{BW}) T_s} = e^{-j\frac{\pi}{OSR}} \approx 1
\]

(2.17)

2) At low frequencies, the STF of a CT \( \Delta \Sigma \) modulator and, equivalently, the magnitude response of \( F_{AA}(s) \) in (2.10) is approximately unity. This results in:

\[
\lim_{f \to 0} |F_{AA}(j2\pi f)| = \lim_{f \to 0} \left| \frac{G(j2\pi f)}{1 + H_{eq}(e^{j2\pi f T_s})} \right| = 1
\]

(2.18)

Substituting (2.1) and (2.13) into (2.18) results in:

\[
\prod_{i=1}^{N} a_i = \prod_{p=1}^{N} |1 - z_p|
\]

(2.19)

Using (2.17) and (2.19), equation (2.16) can be simplified as:

\[
\frac{1}{|F_{AA}(j2\pi f)|} \bigg|_{f=f_{S}-f_{BW}} = \frac{|j2\pi f T_s|^N}{e^{-j\frac{\pi}{OSR}} - 1} \left| \prod_{p=1}^{N} \left( e^{j2\pi f T_s} - z_p \right) \right|_{f=f_{S}-f_{BW}}
\]

(2.20)
Using Euler’s formula, some trigonometric identities, and Taylor’s expansion, equation (2.20) can be further simplified to express the minimum alias suppression as:

\[ MS_{AA} = \left. \frac{1}{|F_{AA}(j2\pi f)|} \right|_{f=f_S-f_{BW}} = (2OSR)^N \]  

(2.21)

This result demonstrates that the minimum alias suppression of the proposed anti-aliasing filter only depends on the OSR and the filter order \( N \).

### 2.4.2 Inband Alias Power

Another way to evaluate the performance of an anti-aliasing filter is to calculate the total signal power that can alias into the input-signal band at the filter output, assuming a normalized signal with a white spectrum at the filter input. This is referred to as the inband alias power, \( P_{\text{alias}} \).

Since signals in the frequency range \( kf_S \pm f_{BW} \) \( (k = 1, 2, \ldots) \) can alias inband, the alias power is given by:

\[ P_{\text{alias}} \equiv \frac{1}{f_{BW}} \sum_{k=1}^{\infty} \int_{(kS-f_{BW})}^{(kS+f_{BW})} |F(j2\pi f)|^2 df \]  

(2.22)

where \( |F(j2\pi f)| \) is the magnitude response of the filter. For the proposed anti-aliasing filter, the inband alias power around \( f_S \) is the major source of inband aliased noise, and can be approximated (using equation (2.22) with \( k = 1 \) ) as:

\[ P_{\text{alias}, AA1} \equiv \frac{1}{f_{BW}} \int_{(S-f_{BW})}^{(S+f_{BW})} |F_{AA}(j2\pi f)|^2 df \approx \frac{2}{2N+1} \left( \frac{1}{2OSR} \right)^{2N} \]  

(2.23)

### 2.4.3 Comparison to Butterworth Filters

Consider a classical \( N \)-th-order low-pass Butterworth filter with a 3-dB corner frequency at the signal-band edge \( f_{BW} \). Its magnitude response is given by:

\[ |F_{\text{BUTT}}(j2\pi f)| = \left| \frac{1}{\sqrt{\left(1 + \left(\frac{f}{f_{BW}}\right)^N\right)}} \right| \]  

(2.24)
When used as an anti-aliasing filter, this Butterworth filter has a minimum alias suppression of:

\[
MS_{\text{BUTT}} = \frac{1}{|F_{\text{BUTT}}(j2\pi(f_s-f_{BW}))|} \approx (2OSR)^N \tag{2.25}
\]

Comparing (2.25) and (2.21) reveals that the proposed anti-aliasing filter has a minimum alias suppression equivalent to a classical Butterworth filter of the same order \(N\). This is shown in Fig. 2.12, where the magnitude responses of the proposed anti-aliasing filter and the Butterworth filter are plotted.

For the Butterworth filter, the inband alias power around \(f_s\) can be approximated as:

\[
P_{\text{alias, BUTT}} = \frac{1}{f_{BW}} \int_{(f_s-f_{BW})}^{(f_s+f_{BW})} |F_{\text{BUTT}}(j2\pi f)|^2 df \approx 2\left(\frac{1}{2OSR}\right)^{2N} \tag{2.26}
\]

Comparing (2.23) and (2.26) reveals that, whereas both filters have the same OSR dependence, the proposed anti-aliasing filter has a factor \(2N+1\) better alias suppression than a Butterworth filter of the same order \(N\). Intuitively, less aliasing (smaller \(P_{\text{alias}}\)) is expected using the proposed anti-aliasing filter, owing to its notches at multiples of \(f_s\). Figure 2.13 compares the inband alias power \(P_{\text{alias}}\) of the proposed anti-aliasing filter and a low-pass Butterworth, computed over the first 10 aliases of the input-signal band (i.e., for \(k=1,\ldots, 10\) in equation (2.22)). Signals beyond these aliases are highly suppressed and, hence, insignificant. As per Fig. 2.13, the proposed anti-aliasing filter achieves more alias suppression (smaller \(P_{\text{alias}}\)) than a Butterworth filter of the same order. Furthermore, its relative performance improves with increasing filter order. Accordingly, the alias suppression advantages of the proposed anti-aliasing filter are most noticeable when designed for higher orders, where it would significantly outperform a Butterworth filter.
One of the most important advantages of the proposed anti-aliasing filter is that it scales with the sampling frequency, thereby enabling its use as a general-purpose IP block. Specifically, starting with a nominal filter design, the input-signal band $f_{BW}$ or the alias suppression can be increased by increasing the sampling frequency $f_S$, without compromising the other filter characteristics (stability, pass-band gain, high-pass shaping of sampling errors), as demonstrated below.

**Figure 2.12** (a) Magnitude response of the proposed anti-aliasing filter $F_{AA}(s)$ and of an equal-order Butterworth filter $F_{BUTT}(s)$ with a 3-dB cutoff frequency at the signal-band edge $f_{BW}$. (b) Zoom-in of the filter responses in (a) around the 1st alias band. ($N = 2, a_1 = 0.325, a_2 = 0.667, OSR = 16$).

### 2.5 Use of the proposed Anti-Aliasing Filter as a General-Purpose IP Block

One of the most important advantages of the proposed anti-aliasing filter is that it scales with the sampling frequency, thereby enabling its use as a general-purpose IP block. Specifically, starting with a nominal filter design, the input-signal band $f_{BW}$ or the alias suppression can be increased by increasing the sampling frequency $f_S$, without compromising the other filter characteristics (stability, pass-band gain, high-pass shaping of sampling errors), as demonstrated below.
Figure 2.13 Inband alias power $P_{\text{alias}}$ (in the first 10 aliases of the input-signal band) versus oversampling ratio OSR, using the proposed anti-aliasing filter and an equal-order lowpass Butterworth filter, for various filter orders.

2.5.1 Filter Stability

The filter performance (minimum alias suppression $MS_{\text{AA}}$ and inband alias power $P_{\text{alias, AA1}}$ in (2.21) and (2.23)) is only a function of the OSR and filter order $N$. By increasing the sampling frequency $f_S$, the filter performance improves for the same signal band $f_{BW}$ (increasing OSR) or is unchanged for a larger $f_{BW}$ (constant OSR). This is provided that any inband signal is not attenuated and the filter remains stable.

To study the filter stability, assume that the sampling frequency is increased from $f_S$ to $f'_S$. Owing to the cascade of integrators (Fig. 2.3a), this does not affect the zeros of $NTF(z)$ in (2.13). However, the poles $z_p$ will shift to new positions $z'_p$. To find the new pole positions $z'_p$, the forward filter $G(s)$ in (2.1) can be re-expressed in terms of $f'_S$ as:

$$G(s) = \frac{1}{(sT'_S)^N} \prod_{i=1}^{N} a'_i$$

(2.27)
Here, the equivalent integrator coefficients \( a_i' = \left( \frac{f_S'}{f_S} \right) a_i \) decrease with increasing \( f_S' \). Consequently, for the DT poles \( z_p' \), equation (2.19) can be expressed in terms of the new DT poles \( z_p' \) as:

\[
\prod_{p=1}^{N} \left| 1 - z_p' \right| = \left( \frac{f_S'}{f_S} \right)^N \prod_{i=1}^{N} a_i
\]  

(2.28)

Accordingly, for increasing sampling frequency \( f_S' \), the poles are drawn to dc (\( z = 1 \)), which corresponds to a stable system. On the other hand, for decreasing sampling frequency \( f_S' \), the poles are pushed away from dc, which may cause instability. This is illustrated in Fig. 2.14. Here, the root locus of \( NTF(z) \) in equation (2.13) is plotted, while the sampling frequency \( f_S \) is increased from 0.25 to 256 times its nominal value \( f_S = f_{S,\text{nom}} \). Observe that, when \( f_S \) is decreased to \( 0.25 f_{S,\text{nom}} \), one pole is outside the unit circle (unstable system) and the other pole is near the origin (stable system). Therefore, decreasing \( f_S \) may lead to instability. On the other hand, increasing \( f_S \) pushes the poles towards \( z = 1 \) (dc) in the limiting case, thereby maintaining stability. Accordingly, to guarantee stability over a broad range of \( f_S \), a good design strategy is to design the nominal filter for the lowest \( f_S \) used.
2.5.2 Sampling-Frequency Range

Figure 2.15a shows the magnitude response of the proposed anti-aliasing filter (Fig. 2.3a with $N = 2$), for a nominal sampling frequency $f_S = f_{S, nom}$. The responses for $f_S = 4f_{S, nom}$ and $f_S = 16f_{S, nom}$ are also shown. To maximize the sampling-frequency range, the nominal poles of $NTF(z)$ in equation (2.13) are placed as far away from dc as possible, without causing any peaking in the magnitude response of the filter (similar to the peaking in the STF of CT ΔΣ modulator [Maeyer, EL05]). This corresponds to $a_1 = 0.7586$ and $a_2 = 1.595$. In Fig. 2.15a, the frequency axis is plotted on a base 2 log scale, such that the input-signal band edges for different OSR values coincide with the grid (i.e., $f_{BW}/f_S = 2^{-(1+\log_{2} OSR)}$).

Observe that in Fig. 2.15a, at $f_S = f_{S, nom}$, the anti-aliasing filter can operate at an $OSR \geq 2$, without attenuating any inband signal. At $f_S = 4f_{S, nom}$, the filter poles will shift closer to dc (as described above) and, hence, the anti-aliasing filter must operate at an $OSR \geq 16$, to avoid attenuating any inband signal. At $f_S = 16f_{S, nom}$, this trend continues and the anti-aliasing filter must operate at an $OSR \geq 64$.

Figure 2.15b shows a magnified version of the filter magnitude responses in Fig. 2.15a around the 1st alias band. The dashed lines indicate the alias-band edges $1 \pm f_{BW}/f_S = 1 \pm 1/(2OSR)$ for various OSRs. This confirms the analysis in Section IV that a maximum OSR is required for optimal performance (in term of minimum alias suppression $MS_{AA}$ and inband alias power $P_{alias}$).

The above observation can be summarized as follows

1) **For a constant input-signal band $f_{BW}$**: the sampling frequency $f_S$ (or, equivalently, the OSR) can be increased arbitrarily, resulting in an improvement of the minimum alias suppression $MS_{AA}$ and inband alias power $P_{alias, AA1}$ (in equations (2.21) and (2.23)) by $6N$ dB per octave, where $N$ is the filter order.

2) **For a constant OSR**: the sampling frequency $f_S$ can be increased, with the
corresponding input-signal band \( f_{BW} \) increased by the same factor (up to \( x16 \) in Fig. 2.15a if the initial input-signal band is \( (f_{BW}/f_{S,nom}) \approx 0.01 \), without attenuating any inband signal.

Accordingly, for a nominal filter design, the input-signal pass-band or the alias suppression can be increased by increasing the sampling frequency, without compromising the other filter characteristics (stability, pass-band gain, shaping of sampling errors). Thus, the proposed anti-aliasing filter is particularly attractive as a general-purpose IP block.
Chapter 3

Behavioral Simulations of the Proposed Anti-Aliasing Filter

3.1 System-Level Nonidealities

Before commencing transistor-level design, the system level specifications are found by modeling the system nonidealities. This allows the designer to predict the filter’s performance and to set circuit block specifications. Specifically, in ΔΣ systems there is no shaping of errors at the input node. Thus, it is vital to model nonidealities at the input of the proposed anti-aliasing filter since they will determine the system’s performance. In this section, the factors that will be discussed are: thermal noise, clock-jitter, and signal-swing levels.

3.1.1 Thermal Noise

Thermal noise is one of the performance limiting nonidealities and is modeled as white noise. It is especially problematic at the input of the filter where it is not shaped, hence, any thermal noise at the input node limits the performance of the anti-aliasing filter in terms of achievable resolution. Furthermore, many ΔΣ systems are designed such that they are dominated by the thermal noise of the first integrator [Ortmanns 06].

The input of the proposed anti-aliasing filter is composed of the integrator and feedback resistors with the associated thermal noise sources as shown in Fig. 3.1 for a fully differential
active-RC integrator [Ortmanns 06]. The total input referred thermal-noise spectrum can be expressed as:

\[
\mathbb{P}_{n,in}^2 = 2\left(\mathbb{P}_{n,R}^2 + \mathbb{P}_{n,\text{RDAC}}^2 \frac{R^2}{R_{\text{DAC}}^2} \right) + \mathbb{P}_{n,\text{OTA}}^2 \left(1 + \frac{R}{R_{\text{DAC}}} \right)^2 \frac{V^2}{Hz} \tag{3.1}
\]

where \(\mathbb{P}_{n,R}\) and \(\mathbb{P}_{n,\text{RDAC}}\) are the thermal noise of the input resistor and feedback DAC resistor, respectively, and \(\mathbb{P}_{n,\text{OTA}}\) is the thermal noise of the OTA.

The thermal noise spectrum of resistors, and the OTA are given by \(4kT R\) and \(4kT \frac{\gamma}{g_{m,\text{OTA}}}\), respectively. Therefore, the total input-referred inband noise power is:

\[
P_N = 8kT f_{bw} \left[ R + \frac{R^2}{R_{\text{DAC}}^2} + \frac{\gamma}{g_{m,\text{OTA}}} \left(1 + \frac{R}{R_{\text{DAC}}} \right)^2 \right] \tag{3.2}
\]

where \(g_{m,\text{OTA}}\) is the transconductance of the OTA, \(\gamma\) is the thermal noise factor, and \(f_{bw}\) is the bandwidth of the filter [Ortmanns 06]. Furthermore, note that \(R/R_{\text{DAC}}\) sets the feedback coefficient of the filter, hence, \(R\) and \(R_{\text{DAC}}\) are dependent on each other.
3.1.2 Clock-Jitter

The effect of the clock jitter introduced in the CT feedback signal is important since it is not shaped by the ΔΣ NTF. The jitter performance of the proposed anti-aliasing filter can be compared to that of a CT ΔΣ modulator, where the inband error power due to jitter \( P_j \) is given by [Samid, ICECS03]:

\[
P_j = \frac{(2V_{REF})^2}{2^B - 1} \left( \frac{\delta_t}{T_S} \right)^2 \frac{\alpha}{OSR}
\]  

(3.3)

Here, \( V_{REF} \) is the reference voltage of the quantizer, \( B \) is the number of quantization bits, \( \delta_t \) is the standard deviation of the clock jitter assuming the jitter is a gaussian random process and the spectrum of the jitter is white, and \( \alpha \) is the activity factor (\( \alpha = 1 \) for NRZ).

Observe that as \( B \) approaches \( \infty \) in (3.3), \( P_j \) tends to 0. Since the proposed anti-aliasing filter can intuitively be seen as having an infinite number of quantization bits, it should have very good jitter performance, limited only by the speed of the sampling operation.

3.1.3 Signal-Swing at the Output of the S/H and First Integrator

The signal-swing at the output of the S/H opamp and the signal-swing at the output of the first integrator, together, set the nonlinearity of the filter since their nonlinearity is not shaped. Higher signal-swings result in larger nonlinearity because the voltage approaches the supply rails causing the dc gain to fluctuate from its peak. Thus, one way to reduce the nonlinearity of the system is to reduce the signal-swing at either the output of the S/H or the output of the first integrator.

The signal-swing at the output of the S/H circuit should be equivalent to the signal-swing at the input of the filter. Since maximizing the input-signal swing increases the dynamic range, then the signal swing at the output of the S/H circuit cannot be changed. However, the signal-swing at the output of the first integrator can be decreased by modifying the feedback coefficients and the coefficients of the integrators. For example, Fig 3.2a shows the initial design of a 2nd-order filter.
Chapter 3: Behavioral Simulations of the Proposed Anti-Aliasing Filter

with the corresponding feedback and integrator coefficients. Observe that if the feedback coefficients \( b_1 \) and \( b_2 \) are 1, then the output swing of both integrators is equal to the input signal-swing. To reduce the output swing of the first integrator by half, but keep the output swing of the S/H the same (i.e., the output of the circuit), then coefficients \( a_1, a_2, \) and \( b_2 \) are modified as shown in Fig. 3.2b. Importantly, this does not alter the STF or NTF response of the filter.

Since the swing at the output of the first integrator can be decreased, thus decreasing the associated nonlinearity, the nonlinearity of the overall filter will be dominated by the S/H opamp. Furthermore, the nonlinear gain of the S/H opamp can be modeled as shown in [Hamoui 04]:

\[
A(v_{out}) = \begin{cases} 
A_{max} \left[ 1 - \left( \frac{v_{out}}{V_{o, sat}} \right)^2 \right] & \text{for } v_{out} \leq V_{o, sat} \\
0 & \text{for } v_{out} > V_{o, sat}
\end{cases}
\]  

(3.4)
where $A_{max}$ is the maximum dc gain, and $V_{o,sat}$ is the output saturation voltage of the opamp. Lastly, this model can be tuned to meet the observations from transistor-level simulations by changing the value of $V_{o,sat}$.

### 3.2 Behavioral Model of the CT Integrator

Consider the CT integrator, with the feedback path in Fig. 3.3. The integrator transfer function (ITF) can be expressed as:

$$\text{ITF}(s) = \frac{1}{sCR\left(1 + \frac{1}{A(s)}\right) + \frac{1}{A(s)}\left(1 + \frac{R}{R_{DAC}}\right)}$$

Observe from (3.5) that if $A(s) \to \infty$, then the ITF reduces to the ideal case of $\frac{1}{sRC}$. However, the opamp is usually modeled as a single pole system [Hamoui, ISLPED06]:

$$A(s) = \frac{A_0}{1 + \frac{s}{\omega_p}}$$

**Figure 3.3** An integrator with an opamp having an open loop transfer function $A(s)$. Modeling the loading effect of resistor $R_{DAC}$ is important since it can cause a noticeable increase in the opamp specifications.
where $A_0$ is the finite gain, and $\omega_p$ is the dominant pole. Therefore, the ITF can now be expressed as:

$$ITF(s) = \frac{GBW/(RC)}{s^2 + s\left[GBW + \omega_p + \frac{1}{RC}\left(1 + \frac{R}{R_{DAC}}\right)\right] + \frac{\omega_p}{RC}\left(1 + \frac{R}{R_{DAC}}\right)}$$

(3.7)

where $GBW = A_0\omega_p$ is the gain-bandwidth product. This model accounts for finite-gain, finite gain-bandwidth, and the loading effect of the feedback resistor, $R_{DAC}$. Opamp nonlinearity in the integrator was not modeled since the system’s linearity is set by the S/H circuit as described in Section 3.1.3.

### 3.3 Behavioral-Simulation Models and Results

#### 3.3.1 Behavioral-Simulation Conditions and Models

The behavioral simulations of a 2nd-order anti-aliasing filter were performed in SIMULINK with the following conditions:

- The filter bandwidth was set to $2MHz$, in order to be used in UMTS applications, and the nominal sampling frequency, $f_{S,nom}$, is set to $32MHz$, resulting in an $OSR = 8$.
- A nonideal zero-order hold is used to account for the nonlinear gain in the S/H opamp, where the output saturation voltage is set to $V_{o,sat} = 1.2V$.
- The thermal noise is modeled at the inputs of both the first and second integrators, and is assumed to be dominated by the resistors $R$ and $R_{DAC}$ in Fig. 3.3.
- Where applicable, the input signal is set to $200kHz$, in order for the third and fifth order harmonics to fall inband.
- The overall filter is designed for $SNDR > 68dB$ (12 bits of resolution).

Therefore, the behavioral models in SIMULINK account for finite dc gain and finite gain-bandwidth in the integrator opamps, finite gain and nonlinear gain in the S/H, and thermal noise in
Chapter 3: Behavioral Simulations of the Proposed Anti-Aliasing Filter

3.3.2 Clock-Jitter Simulation

Figure 3.4 plots $P_j$ (described in Section 3.1.2) versus input frequency for CT $\Delta \Sigma$ modulators with $B$-bit quantizers (-) and the proposed anti-aliasing filter (*). ($f_s = 200$ MHz, $OSR = 64$, $a_1 = 0.667$, $a_2 = 1.5$, $b_1 = b_2 = 1$, and $\delta_t/T_s = 0.1$)

Figure 3.4 Inband error power due to jitter versus input frequency for CT $\Delta \Sigma$ modulators with $B$-bit quantizers (-) and the proposed anti-aliasing filter (*). ($f_s = 200$ MHz, $OSR = 64$, $a_1 = 0.667$, $a_2 = 1.5$, $b_1 = b_2 = 1$, and $\delta_t/T_s = 0.1$)

the first and second integrators. Clock-jitter is dealt separately in the following section (3.3.2) since its effects are found to be negligible.

3.3.2 Clock-Jitter Simulation

Figure 3.4 plots $P_j$ (described in Section 3.1.2) versus input frequency for both CT $\Delta \Sigma$ modulators and the proposed anti-aliasing filter (using the SIMULINK jitter models that were developed in [Chopp, TCASI09]). For inband frequencies, the proposed filter has the jitter performance equivalent to that of a CT $\Delta \Sigma$ modulator with a 13-bit quantizer. Moreover, the proposed filter has lower $P_j$ than the 13-bit quantizer at frequencies around multiples of $f_s$. Thus, the proposed filter has good jitter performance especially when compared to that of a typical CT $\Delta \Sigma$ modulator ($B = 1 \ldots 5$).
3.3.3 Requirements on Filter Coefficients

The filter coefficients can be designed to give the desirable STF and NTF responses. Observe that the required bandwidth of the filter is \(2MHz\). However, the filter should not necessarily be designed to have its 3dB cutoff frequency at \(2MHz\). This is because the NTF will then only shape noise up to \(2MHz\), and since this is inband, the filter will not possess the advantage of noise-shaping errors. Therefore, the filter coefficients should be designed to obtain a cutoff frequency that is higher than \(2MHz\). Hence, the initial coefficients were chosen to be \(a_1 = 0.4\), \(a_2 = 0.75\), \(b_1 = 1\), and \(b_2 = 1\). However, due to the need to decrease the signal swing at the output of the first integrator (as explained in section 3.1.3), the coefficients are modified to \(a_1 = 0.2\), \(a_2 = 1.5\), \(b_1 = 1\), and \(b_2 = 0.5\).

In the ideal case, these coefficients result in a 3dB corner frequency of 3.8MHz, where the sampling frequency is equal to the nominal sampling frequency \(f_S = f_{S,\text{nom}}\). However, to take advantage of the filter’s properties, the filter was also tested at up to 4-times the nominal sampling frequency. Figure 3.5 shows the ideal filter response, near the 3dB point, for OSR values up to 32 \(f_S = 128MHz\). The 3dB frequency remains above the targeted cutoff of 2MHz thus demonstrating that the coefficients are well chosen. However, the slight shift in the curve also signifies a slightly less aggressive NTF leading to less shaping of errors.

3.3.4 Requirements on Opamp Gain and Gain-Bandwidth

The dc gain of the integrator opamps can be set by checking the STF response of the filter. Specifically, it is observed that the notch depth is directly dependent on the dc gain of both opamps. For example, Fig 3.6a shows the STF response at the first notch, for the same GBW but differing dc gains. However, the notch depth is ultimately limited irrespective of the dc gains. This is due to the system’s noise floor (usually dominated by thermal noise), and thus, it suffices to set the opamp gains to 100.
Chapter 3: Behavioral Simulations of the Proposed Anti-Aliasing Filter

The GBW is be set by checking the STF response near the 3dB cutoff as shown in Fig. 3.6b. Assuming that up to 5% error in the 3dB cutoff can tolerated, and that the second opamp can scale by a factor of 2, then the GBW of the first and second opamp can be set at approximately 200 MHz, and 100MHz, respectively. Designing for a higher GBW would require more power and not significantly change the STF response.

The GBW is be set by checking the STF response near the 3dB cutoff as shown in Fig. 3.6b. Assuming that up to 5% error in the 3dB cutoff can tolerated, and that the second opamp can scale by a factor of 2, then the GBW of the first and second opamp can be set at approximately 200 MHz, and 100MHz, respectively. Designing for a higher GBW would require more power and not significantly change the STF response.

The S/H opamp can be designed based on the size of the harmonic distortion terms due to the nonlinearity. Furthermore, the opamp needs to be able to settle within approximately $T_s/4$ since this is how long the S/H opamp is connected in feedback according to the timing of the switches. Thus, the maximum sampling frequency sets the gain-bandwidth of the S/H opamp.
3.3.5 Overall Behavioral-Simulation Results

The dynamic range plot of the designed 2nd-order anti-aliasing filter is shown in Fig. 3.7. The specifications used during the simulations are summarized in Table 3.1. Based on the behavioral simulations, the DR is found to be 71dB, while the peak SNDR is found to be 66.4dB. The bits of resolution is defined as [Hamoui 04]:

\[ N_B \equiv \frac{DR_{dB} - 1.76}{6.02} = 11.5 \]  

and, hence, the filter has 12 bits of resolution.

Figure 3.6 (a) Notch depth at \( f_S \) for differing dc gains, \( A_0 \), (but constant GBW) in the integrator opamps. Observe that ultimately, the notch depth is limited by the thermal noise floor of the whole system. (b) Magnitude response of the proposed filter with differing GBW values. Observe that in each simulation \( GBW_2 = 0.5GBW_1 \). It was found that increasing \( GBW_1 \) above 200 MHz resulted in little improvement in the magnitude response, but would require more power. \( (a_1 = 0.2, a_2 = 1.5, b_1 = 1, b_2 = 0.5) \)
Table 3.1 Specifications for the final behavioral simulations of the proposed filter.

<table>
<thead>
<tr>
<th>Component</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Integrator 1</td>
<td>$GBW = 200\text{MHz}$</td>
</tr>
<tr>
<td></td>
<td>$A_0 = 100$</td>
</tr>
<tr>
<td></td>
<td>$R = 20k\Omega$</td>
</tr>
<tr>
<td></td>
<td>$R_{DAC} = 20k\Omega$</td>
</tr>
<tr>
<td>Integrator 2</td>
<td>$GBW = 100\text{MHz}$</td>
</tr>
<tr>
<td></td>
<td>$A_0 = 100$</td>
</tr>
<tr>
<td></td>
<td>$R = 12k\Omega$</td>
</tr>
<tr>
<td></td>
<td>$R_{DAC} = 35k\Omega$</td>
</tr>
<tr>
<td>S/H Opamp</td>
<td>$A_{\text{max}} = 150$</td>
</tr>
<tr>
<td></td>
<td>$V_{o,\text{sat}} = 1.2V$</td>
</tr>
</tbody>
</table>

Figure 3.7 Behavioral simulation, including nonidealities, of the proposed 2nd-order filter. From the graph: $DR = 71\text{dB}$, $SNDR_{\text{peak}} = 66.4\text{dB}$, and $N_B = 11.5$. 
Chapter 4

Circuit-Level Design and Simulation of the Proposed Anti-Aliasing Filter

4.1 Noise Budget

The resolution of the proposed anti-aliasing filter is limited by the thermal noise from the input and feedback resistors of the integrators, and by the nonlinear gain from the S/H opamp. For 12-bits of resolution, the SNDR must be 74dB and is given by:

\[ \frac{P_s}{P_n} = 10^{SNDR/10} \]  

(4.1)

where \( P_s \) is the input signal power, and \( P_n \) is the total inband noise power. Furthermore, assuming that the input signal is \( 1V_{pp} \) then in order for \( SNDR = 74dB \), the total inband noise power must be \( P_n = 4.98 \times 10^{-9} V^2 \). The noise contribution can be split approximately evenly as shown in Table 4.1. Assuming that the second integrator does not contribute a significant amount of thermal noise (due to shaping) then resistors \( R \), and \( R_{DAC} \) of the first integrator can have a maximum value of 20kΩ each.

Table 4.1  Noise sources can be reduced to just the nonlinear gain of the S/H opamp and the thermal noise from the input resistors.

<table>
<thead>
<tr>
<th>Error Source</th>
<th>Inband Noise Power (nV^2)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Nonlinear Opamp Gain (S/H circuit)</td>
<td>2.35</td>
</tr>
<tr>
<td>Thermal Noise</td>
<td>2.65</td>
</tr>
<tr>
<td>Total</td>
<td>5</td>
</tr>
</tbody>
</table>
Finally, Table 4.2 lists the minimum opamp specifications for the integrators and S/H, once again assuming $V_{in} = 1V_{pp}$. The gain-bandwidth product of the third opamp is set by assuming $f_{S,nom} = 32MHz$, and that the S/H circuit needs three time constants to settle within a period of $0.25/f_{S,nom}$.

### 4.2 Opamp Design

The opamp configuration chosen was a classical two-stage opamp as shown in [Johns 97]. This opamp is sufficient for this application because of its moderate gain and large output swing, which allows for the opamp specifications in Chapter 3 to be easily met. Also, this opamp uses a compensation capacitor which is needed for the opamp in the S/H circuit. The opamp circuit diagram is shown in Fig. 4.1 and includes the common mode feedback (CMFB) circuit which is based on [Henkel, JSSC02]. The CMFB circuit is a low gain opamp that senses the average output level, compares it to the reference, and then accordingly modifies the gate voltage of $M_3$ and $M_4$. The CMFB has a negative feedback and works well as long as $v_{gs}$ of $M_{12-13}$ is close to the expected $v_{gs}$ of $M_{3-4}$.

Table 4.2 Minimum opamp specifications for the proposed 2nd-order anti-aliasing filter.

<table>
<thead>
<tr>
<th>Specification</th>
<th>First Opamp (Integ. 1)</th>
<th>Second Opamp (Integ. 2)</th>
<th>Third Opamp (S/H)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Total load capacitance</td>
<td>N/A</td>
<td>1 pF</td>
<td>N/A</td>
</tr>
<tr>
<td>Total load resistance</td>
<td>20 kΩ</td>
<td>N/A</td>
<td>20 kΩ</td>
</tr>
<tr>
<td>Differential output voltage swing amplitude</td>
<td>250 mV</td>
<td>500 mV</td>
<td>500 mV</td>
</tr>
<tr>
<td>DC gain (with load)</td>
<td>40 dB</td>
<td>40 dB</td>
<td>43 dB</td>
</tr>
<tr>
<td>Gain-bandwidth product</td>
<td>200 MHz</td>
<td>100 MHz</td>
<td>384 MHz</td>
</tr>
<tr>
<td>Phase margin</td>
<td>70°</td>
<td>70°</td>
<td>70°</td>
</tr>
</tbody>
</table>

Finally, Table 4.2 lists the minimum opamp specifications for the integrators and S/H, once again assuming $V_{in} = 1V_{pp}$. The gain-bandwidth product of the third opamp is set by assuming $f_{S,nom} = 32MHz$, and that the S/H circuit needs three time constants to settle within a period of $0.25/f_{S,nom}$.
swing. Finally, tables 4.4 and 4.5 list the transistor and other component sizes for each opamp. Observe that the CMFB transistor sizes are different for all three opamps because $v_{gs}$ of $M_{3-4}$ is slightly different for each opamp.

![Fully differential two-stage opamp with CMFB.](image)

**Figure 4.1** Fully differential two-stage opamp with CMFB.

<table>
<thead>
<tr>
<th>Specification</th>
<th>First Opamp</th>
<th>Second Opamp</th>
<th>Third Opamp</th>
</tr>
</thead>
<tbody>
<tr>
<td>Total Load Resistance</td>
<td>20 kΩ</td>
<td>N/A</td>
<td>12 kΩ</td>
</tr>
<tr>
<td>Total Load Capacitance</td>
<td>N/A</td>
<td>1 pF</td>
<td>N/A</td>
</tr>
<tr>
<td>Differential output voltage swing amplitude</td>
<td>250 mV</td>
<td>500 mV</td>
<td>500 mV</td>
</tr>
<tr>
<td>Input and output common mode voltage</td>
<td>600 mV</td>
<td>600 mV</td>
<td>600 mV</td>
</tr>
<tr>
<td>DC Gain (with load), $A_0$</td>
<td>40.38 dB</td>
<td>40.58 dB</td>
<td>43.64 dB</td>
</tr>
<tr>
<td>Unity-gain frequency, $f_f$</td>
<td>248 MHz</td>
<td>104 MHz</td>
<td>420 MHz</td>
</tr>
<tr>
<td>Phase margin</td>
<td>66°</td>
<td>62°</td>
<td>66°</td>
</tr>
<tr>
<td>Power consumption</td>
<td>290 µW</td>
<td>320 µW</td>
<td>590 µW</td>
</tr>
</tbody>
</table>
Table 4.4  Transistor sizes for each opamp based on Fig. 4.1.

<table>
<thead>
<tr>
<th>Opamp</th>
<th>M_{1,2}</th>
<th>M_{3,4}</th>
<th>M_{5}</th>
<th>M_{6,7}</th>
<th>M_{8,9}</th>
<th>M_{10,11}</th>
<th>M_{12,13}</th>
<th>M_{14}</th>
<th>M_{15}</th>
</tr>
</thead>
<tbody>
<tr>
<td>Opamp 1</td>
<td>18</td>
<td>9</td>
<td>5</td>
<td>5</td>
<td>20</td>
<td>15</td>
<td>2.3</td>
<td>1.3</td>
<td>5</td>
</tr>
<tr>
<td>W (μm)</td>
<td>18.00</td>
<td>9.00</td>
<td>5.00</td>
<td>5.00</td>
<td>20.00</td>
<td>15.00</td>
<td>2.30</td>
<td>1.30</td>
<td>5.00</td>
</tr>
<tr>
<td>L (μm)</td>
<td>0.18</td>
<td>0.18</td>
<td>0.10</td>
<td>0.10</td>
<td>0.15</td>
<td>0.18</td>
<td>0.18</td>
<td>0.10</td>
<td>0.10</td>
</tr>
<tr>
<td>Opamp 2</td>
<td>18</td>
<td>9</td>
<td>4</td>
<td>6</td>
<td>20</td>
<td>15</td>
<td>2.7</td>
<td>1.2</td>
<td>5</td>
</tr>
<tr>
<td>W (μm)</td>
<td>18.00</td>
<td>9.00</td>
<td>4.00</td>
<td>6.00</td>
<td>20.00</td>
<td>15.00</td>
<td>2.70</td>
<td>1.20</td>
<td>5.00</td>
</tr>
<tr>
<td>L (μm)</td>
<td>0.15</td>
<td>0.15</td>
<td>0.10</td>
<td>0.10</td>
<td>0.12</td>
<td>0.15</td>
<td>0.15</td>
<td>0.10</td>
<td>0.10</td>
</tr>
<tr>
<td>S/H Opamp</td>
<td>25</td>
<td>12.5</td>
<td>10</td>
<td>10</td>
<td>30</td>
<td>15</td>
<td>1.7</td>
<td>1.3</td>
<td>5</td>
</tr>
<tr>
<td>W (μm)</td>
<td>25.00</td>
<td>12.50</td>
<td>10.00</td>
<td>10.00</td>
<td>30.00</td>
<td>15.00</td>
<td>1.70</td>
<td>1.30</td>
<td>5.00</td>
</tr>
<tr>
<td>L (μm)</td>
<td>0.20</td>
<td>0.20</td>
<td>0.10</td>
<td>0.10</td>
<td>0.15</td>
<td>0.18</td>
<td>0.18</td>
<td>0.10</td>
<td>0.10</td>
</tr>
</tbody>
</table>

Table 4.5  Other component sizes for each opamp based Fig. 4.1.

<table>
<thead>
<tr>
<th>Opamp</th>
<th>C_{C} (fF)</th>
<th>R_{Z} (Ω)</th>
<th>R_{1} (kΩ)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Opamp 1</td>
<td>300</td>
<td>600</td>
<td>100</td>
</tr>
<tr>
<td>Opamp 2</td>
<td>600</td>
<td>500</td>
<td>100</td>
</tr>
<tr>
<td>S/H Opamp</td>
<td>350</td>
<td>450</td>
<td>100</td>
</tr>
</tbody>
</table>
4.3 Loop Filter Design

Using the opamps from Section 4.2, the loop filter was designed with the coefficients specified in Fig. 3.5, \( a_1 = 0.2 \), \( a_2 = 1.5 \), \( b_1 = 1 \), and \( b_2 = 0.5 \). For example, to set \( C_1 \):

\[
\frac{1}{a_1 f_S} = R_1 C_1
\]

(2.2)

where \( R_1 \) is set to 20 k\( \Omega \) because of thermal noise considerations. Recalling the swing issues from Section 3.1.3, the trade-off for lowering the output swing of the first integrator (by decreasing \( a_1 \)) is the increased size of capacitor \( C_1 \). The overall loop filter, composed of two integrators, is shown in Fig. 4.2. The corresponding component values are listed in Table. 4.6.

![Figure 4.2](image)

**Figure 4.2** The loop filter of the proposed second-order filter.

<table>
<thead>
<tr>
<th>R_1 (k( \Omega ))</th>
<th>R_{DAC1} (k( \Omega ))</th>
<th>C_1 (pF)</th>
<th>R_2 (k( \Omega ))</th>
<th>R_{DAC2} (k( \Omega ))</th>
<th>C_2 (pF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>20</td>
<td>20</td>
<td>7.81</td>
<td>11.9</td>
<td>35.7</td>
<td>1.75</td>
</tr>
</tbody>
</table>
4.4 Clock Generator Circuit

The clock generator circuit employed is from [Hamoui 04]. However, extra logic blocks are added to generate clocks $\phi_{1A}$, $\phi_{1Ad}$, $\phi_{1B}$, and their inverses, as shown in Fig. 4.3. Particularly, a D flip-flop is used to divide the clock by half, since the faster clock is needed to generate $\phi_{1A}$, $\phi_{1Ad}$, $\phi_{1B}$, and their inverses.

Inverter d is used to set the non-overlap time between clocks $\phi_1$ and $\phi_2$, and between $\phi_{1A}$ and $\phi_{1B}$. Inverter D sets a delay $t_D$ that generates the delayed version of the clocks ($\phi_{1d}$, $\phi_{2d}$, and $\phi_{1Ad}$). Therefore, the non-overlap time between a delayed clocked ($\phi_{1d}$, $\phi_{2d}$, or $\phi_{1Ad}$) and the non-delayed version($\phi_1$, $\phi_2$, or $\phi_{1A}$) is given by:

$$T_{NOV} = t_r + 4t_d - 2t_D$$

where $t_r$ is the rise time of the NOR gate, and $t_d$ is the delay time of inverter d. Observe, that the transmission gates, TG, are designed to have the same delay as D in order to align the each clock with its respective inverse. Finally, the clocks are all buffered by the inverter B in order to set the rise and fall times $T_{R}$.

It is also made sure that the rising and falling edges of the modified clocks coincide with the proper rising and falling edges of the normal clocks. For example, the rising and falling edges of $\phi_1$ coincide with the rising edge of $\phi_{1A}$ and the falling edge of $\phi_{1B}$, respectively. The sizes of the transistors used in each block are listed in Table 4.7. The details of the clocks generated are shown in Fig. 4.4.

<table>
<thead>
<tr>
<th>Table 4.7</th>
<th>Transistor sizes for cells in the clock generator.</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>inv</td>
</tr>
<tr>
<td>PMOS</td>
<td></td>
</tr>
<tr>
<td>$W(\mu m)$</td>
<td>$L(\mu m)$</td>
</tr>
<tr>
<td>NMOS</td>
<td></td>
</tr>
<tr>
<td>$W(\mu m)$</td>
<td>$L(\mu m)$</td>
</tr>
</tbody>
</table>
Figure 4.3 Clock generator circuit including the extra clocks needed to the modified integrator.
Figure 4.4  Clock waveform details based on the clock generator circuit in Fig. 4.3.
4.5 Bootstrapped Switch

Bootstrapped switches have two main advantages: 1) a constant on-resistance and hence very low nonlinearity, and 2) ability to handle high signal swings which also increases the dynamic range of the whole system [Hamoui 04]. The input switch (S₁ in Fig. 2.7) sees a high input swing, but nonlinearity from this switch is also shaped (see section 4.7.1). However, in order to guarantee proper operation, S₁ is bootstrapped such that it can handle high input voltage swings. The idea of a bootstrapped switch, as illustrated in Fig. 4.5a, is to pre-charge the capacitor \( C_B \) to the supply voltage \( V_{DD} \) when the switch is off. Hence, when the switch is turned on \( v_{gs} = V_{DD} \), allowing \( v_{gs} \) to be independent of the input signal, resulting in high linearity and allowing for higher input swings (and consequently higher dynamic range). The bootstrap switch used is from [Dessouky, JSSC01]. The circuit diagram is illustrated in Fig. 4.5b with the associated component sizes in Table 4.8. The switch is tested and its total harmonic distortion (THD) up to the 7th harmonic is found to be \(-95\,dB\), and the on-resistance was found to be 480\,\Omega, at an input amplitude of 300\,mV.
Figure 4.5 Bootstrap switch (a) During the off phase $C_B$ is charged to $V_{DD}$, and $M_0$ is off. During the on phase $v_{gs} = V_{DD}$ thus keeping the on-resistance independent of the input signal. (b) Implementation of the bootstrap switch based on [Dessouky, JSSC01].

Table 4.8 Component sizes of bootstrap switch in Fig. 4.5.

<table>
<thead>
<tr>
<th></th>
<th>$M_0$</th>
<th>$M_{1-9}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$W$ (μm)</td>
<td>0.4</td>
<td>0.2</td>
</tr>
<tr>
<td>$L$ (μm)</td>
<td>0.1</td>
<td>0.1</td>
</tr>
</tbody>
</table>
4.6 Transmission Gate Switch

Switches that do not experience very high input swing can be implemented as transmission gates, as in Fig. 4.6. The THD of the transmission gate up to the 7th harmonic was simulated (as shown in Fig. 4.7) to be $-76\,\text{dB}$ at an input amplitude of 300mV. The on-resistance was found to be highly dependent on the input signal with a peak of $2.8\,\text{k}\Omega$ based on an input amplitude of 300mV.
4.7 Circuit-Simulation Results

4.7.1 Verifying the Shaping of the Sampling Errors by the Proposed Filter

To confirm that sampling errors are shaped, the 1st-order anti-aliasing filter in Fig. 4.8b is simulated in Cadence with sampling switch S₁ replaced by a nonlinear switch, in this case an NMOS transmission gate, while all the other switches are kept ideal. Each opamp was modeled as a simple voltage controlled voltage source as shown in Fig. 4.8c. Since the nonlinear switch generates large harmonics, the magnitude of the harmonics can be compared between the S/H (Fig. 4.8a) and the 1st-order anti-aliasing filter (Fig. 4.8b). It is expected that the harmonics generated by switch in the 1st-order anti-aliasing filter will be attenuated, due to the noise-shaping properties of the delta-sigma loop.
Figure 4.8  Simulation setup to verify the shaping of the sampling errors from switch $S_1$: (a) in a S/H and (b) in a 1\textsuperscript{st}-order anti-aliasing filter (Fig. 2.3a, $a_1 = R/R_{DAC}$) where the S/H in (a) is used. Here the opamps are modeled as shown in (c). The gains of the voltage-controlled voltage sources ($A_1$, $A_2$, and $A_3$) are set at very high values (as given in Table 4.9) in order to approximate an ideal integrator and S/H circuit.
Chapter 4: Circuit-Level Design and Simulation of the Proposed Anti-Aliasing Filter

Table 4.9  Component sizes and gain factors, of the simulation setup in Fig. 4.8, used to verify the shaping of sampling errors. An \( f_S = 1/(RC) = 32\, MHz \) is assumed.

<table>
<thead>
<tr>
<th>R (k( \Omega ))</th>
<th>( R_{DAC} ) (k( \Omega ))</th>
<th>( C ) (pF)</th>
<th>( C_S ) (pF)</th>
<th>( C_C ) (pF)</th>
<th>( A_1 )</th>
<th>( A_2 )</th>
<th>( A_3 )</th>
</tr>
</thead>
<tbody>
<tr>
<td>31.25</td>
<td>31.25</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>10^4</td>
<td>10^4</td>
<td>10^4</td>
</tr>
</tbody>
</table>

Figure 4.9  Circuit-simulation results showing the attenuation of the harmonic magnitudes in the 1\(^{st}\)-order anti-aliasing filter (Fig. 4.8b), compared to the harmonic magnitudes in the S/H circuit of Fig. 4.8a. The attenuation matches well with the expected attenuation obtained from the NTF of a 1\(^{st}\)-order \( \Delta \Sigma \) modulator.

Table 4.9 gives the values used in the simulation setup in Fig. 4.8. Figure 4.9 shows the difference in harmonic magnitudes, at the output of the sampling switch \( S_1 \), between the S/H circuit used as a standalone block (Fig. 4.8a) and when the same S/H circuit is in the 1\(^{st}\)-order anti-aliasing filter, along with the NTF curve of an ideal-first order \( \Delta \Sigma \) modulator (-20dB/dec line). Accordingly, shaping of the sampling errors in the proposed anti-aliasing filter (Fig. 2.3b) corresponds to that of the quantization noise in a \( \Delta \Sigma \) modulator of the same order.
4.7.2 Overall Circuit-Simulation Results

The transistor level design of the circuit was performed in Cadence using 90-nm CMOS technology. The transistor-level simulations were performed using SPECTRE. The switches used were ideal in order to decrease the simulation time and to observe the influence of the nonideal opamps on the magnitude response of the filter.

The magnitude response of the filter was determined by simulating the circuit at various frequencies and comparing the results to the nonideal behavioral models (Section 3.3) and ideal behavioral models (Section 2.2), as shown in Fig. 4.10. Observe that the behavioral models match the transistor level models well. In the simulations, the depth of the notches is limited by the noise floor from the sampling operations. However, since the circuit is designed to be thermal noise dominated, then in practice, the thermal noise would ultimately limit the depth of the notches.
According to noise simulations, the total input referred noise was 18nV$^2$, while according to transient simulations, the THD at 500mV amplitude was 5nV$^2$ giving a total noise of 23nV$^2$. The reason for the disparity between the design and the actual results is that the model did not account for flicker noise, which was found to have a very high corner frequency. Importantly, noise from the sampling operation was found to be negligible, therefore flicker and thermal noise set the filter’s performance. The peak SNDR was found to be 67.4 dB. Furthermore, the dynamic range can be estimated at 72dB based on the relationship between the SNDR and dynamic range from the behavioral simulations (Section 3.3.5). Therefore, the FOM specified in Chapter 1, equation (1.1), is found to be 571. Fig. 4.11 shows how it compares to the other filter designs listed in Table 1.1.

![Figure 4.11 Plot of FOM versus supply voltage, showing how this work compares to other recently published designs.](image-url)
5.1 Summary

A novel anti-aliasing filter that incorporates a sampler has been proposed. Compared to a Butterworth filter of the same order, the proposed filter has the same minimal alias suppression and a higher overall alias suppression (owing to the notches in its magnitude response at multiples of the sampling frequency). In addition, the proposed filter high-pass shapes the sampling errors, similar to the shaping of quantization noise in ΔΣ modulators. Its performance advantages (alias suppression and sampling-error high-pass shaping) increase, as its order or oversampling ratio increases. Furthermore, the input-signal pass-band or the alias suppression of the proposed sampling anti-aliasing filter can be increased by increasing its sampling frequency, without compromising its other characteristics (stability, pass-band gain, sampling-error shaping). Thus, the proposed sampling anti-aliasing filter is particularly attractive as a general-purpose IP block for use at the input of oversampling discrete-time ΔΣ modulators.

5.2 Future Work

Since the S/H circuit requires an opamp, the filter order is one less than the number of opamps. Therefore, the power per pole is significantly higher, especially due to the strict settling requirements of the S/H opamp. Future work can explore higher order filter implementation, where the extra power from the S/H circuit is not as significant. Furthermore, other S/H circuits can be
explored that can also be integrated with the DT integrator. Differing feedback pulse shapes can also be used, hence, the discrete-to-continuous transition need not be strictly implemented as a ZOH.

One of the main advantages of the proposed filter is the notches at the sampling frequency. However, the depth of these notches is ultimately limited by nonidealities such as thermal noise. Future work can explore the trade-off between the depth of the notch and factors such as thermal noise. For example, lowering the thermal noise would require smaller resistors in the integrator which in turn affects the dc gain of the proceeding opamp. Such trade-off need to be explored in order to fully optimize the design.

Finally, to fully compare this proposed anti-aliasing filter to other possible implementations, all the implementations should be designed at the transistor level and compared in terms of power, alias suppression, or other FOMs. Furthermore, the implementations should be designed in conjunction with a simple DT ΔΣ modulator in order to verify common design trade-off such as power and alias attenuation.
References

A


B


C


H


J


K

L


M


