High-Speed Data Transmission Using Substrate Integrated Waveguide-Type Interconnects

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Abstract

Electronic circuits have evolved into multifunctional and highly integrated systems that often require ultra-high-speed and wideband data transmission. Due to the miniaturization trend in CMOS devices, digital processors can now achieve these extreme specifications and enable operation with multi-gigahertz clock frequencies. However, fundamental interconnect limitations prevent from full accomplishment of multi-Gigabit per second data rates. Most importantly, increased conductor and dielectric losses at high frequencies can significantly reduce the channel bandwidth. In addition, crosstalk and electromagnetic interference further deteriorate the link performance, especially in compact routing networks. Therefore, alternative interconnects that enable ultra-high-speed/high-frequency signaling while maintaining signal integrity are needed.

This thesis proposes a new method of high-speed data transfer by utilizing waveguide-type interconnects, which offer efficient and confined data transmission due to their low-loss and excellent isolation properties. The electromagnetic bandgap concept is employed for a systematic design of the waveguide sidewalls in order to yield negligible signal leakage in straight and meandered interconnect paths. The performance of the suggested waveguide interconnects is fully investigated from the signal integrity point of view. Due to the three-dimensional nature of the waveguide and its incompatibility with planar structures, a few transition structures are investigated, and important design parameters are identified. Models for transition structures used in 3-D integration, i.e., the via and aperture transitions, are proposed in order to enable global circuit simulations. Due to the bandpass characteristic of the waveguide channel, modified driver and receiver blocks are introduced to accommodate high-speed baseband signaling, and the first all electrical high-speed serial data transmission system using a substrate integrated waveguide is implemented. Excellent transmission quality is demonstrated experimentally up to a data rate of 5 Gb/s achieving bit error ratio of better than $10^{-13}$. Furthermore, to compensate for the relatively larger footprint occupied by the waveguide compared to conventional printed lines, a substrate reuse approach is proposed by inserting additional lowpass channels inside the waveguide. This hybrid technique proves to increase the aggregate transmission capacity (to 15 Gb/s) by simultaneously utilizing the lowpass and bandpass channels. Finally, an alternative parallel data transmission system is introduced by harnessing multimode transmission through the same waveguide channel and using mode orthogonality. A number
of transition structures and mode launchers to excite and retrieve $\text{TE}_{10}$ and $\text{TE}_{20}$ modes are presented. Experimental characterizations demonstrate excellent transmission quality through the dual-channel system for a data rate of 1 Gb/s/channel.
Abrégé

Les circuits électroniques ont évolué pour devenir des systèmes multifonctionnels hautement intégrés requérant une transmission à très haute vitesse et de large bande. Du à la tendance de miniaturisation des composantes CMOS, les processeurs digitaux peuvent maintenant atteindre ces spécifications extrêmes et permettent par le même fait une opération à plusieurs gigahertz. Cependant, des limitations fondamentales par rapport aux interconnections empêchent une transmission de plusieurs Gigabits par seconde. Plus précisément, la croissance des pertes de conductions et diélectriques aux hautes fréquences peuvent réduire la bande de transmission de façon significative. De plus, la diaphonie et l’interférence électromagnétique contribuent également à détériorer la performance de lien, plus spécialement dans des réseaux de routage compacts. Par conséquent, une alternative aux interconnections standards est nécessaire qui permet une transmission à des fréquences ultra-rapide tout en maintenant l’intégrité des signaux.

Cette thèse propose une méthode nouvelle de transmission de données à haute vitesse utilisant des interconnections à guide d’ondes permettant ainsi une transmission de données efficace grâce aux pertes relativement basses et excellentes propriétés d’isolation. Le concept de bande électromagnétique interdite est utilisé pour un design systématique des parois du guide d’ondes afin de procurer une fuite de signal négligeable dans des interconnections droites ou courbées. La performance de l’interconnexion à guide d’ondes suggérée est complètement investiguée du point de vue de l’intégrité du signal. Du fait de la nature tridimensionnelle du guide d’ondes et son incompatibilité avec les structures planes, quelques structures de transitions sont investiguées et les paramètres cruciaux de design sont identifiés. Des modèles de structures de transitions utilisées dans l’intégration 3-D, les transitions de via et d’aperture, sont proposés afin de permettre la simulation de circuits globales. Du fait de la caractéristique bande-passante du canal guide d’ondes, des blocs de transmetteur et récepteur sont introduits pour accommoder la signalisation à haute vitesse de la bande de base ainsi que le tout premier système de transmission en série à haute vitesse entièrement électrique utilisant un guide d’ondes intégré au substrat. Une transmission de qualité est démontrée expérimentalement jusqu’à des vitesses de 5 Gb/s ayant un taux d’erreurs binaires en dessous de $10^{-13}$. De plus, afin de compenser pour l’aire plus large occupée par le guide d’ondes comparativement aux lignes imprimées conventionnelles, une approche de réutilisation du substrat est proposée en insérant des canaux passe-bas à
l’intérieur du guide d’ondes. Il a été démontré que cette technique hybride accroît la capacité de transmission du canal jusqu’à 15 Gb/s en utilisant simultanément les canaux passe-bas et passe-bandes. Finalement, un système alternatif de transmission en parallèle de données est introduit en attachant la transmission multimodale au même canal à guide d’ondes et en utilisant l’orthogonalité modal. Un nombre de structures de transition et des lanceurs de modes pour exciter et recevoir les modes TE_{10} et TE_{20} sont présentés. Une caractérisation expérimentale démontre une excellente qualité de transmission par le système double-canal pour une vitesse de 1 Gb/s/canal.
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<thead>
<tr>
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<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>2-D</td>
<td>Two-Dimensional</td>
</tr>
<tr>
<td>3-D</td>
<td>Three-Dimensional</td>
</tr>
<tr>
<td>4-PAM</td>
<td>Four-Level Pulse Amplitude Modulation</td>
</tr>
<tr>
<td>16-QAM</td>
<td>16-Point Quadrature Amplitude Modulation</td>
</tr>
<tr>
<td>ACCI</td>
<td>Alternative Current Coupled Interconnect</td>
</tr>
<tr>
<td>ADC</td>
<td>Analog-to-Digital Converter</td>
</tr>
<tr>
<td>BER</td>
<td>Bit Error Ratio</td>
</tr>
<tr>
<td>BGA</td>
<td>Ball Grid Array</td>
</tr>
<tr>
<td>BPSK</td>
<td>Binary Phase Shift Keying</td>
</tr>
<tr>
<td>CDMA</td>
<td>Code Division Multiple Access</td>
</tr>
<tr>
<td>CPW</td>
<td>Coplanar Waveguide</td>
</tr>
<tr>
<td>DLL</td>
<td>Delay Locked Loop</td>
</tr>
<tr>
<td>EBG</td>
<td>Electromagnetic Bandgap</td>
</tr>
<tr>
<td>EMI</td>
<td>Electromagnetic Interference</td>
</tr>
<tr>
<td>FDMA</td>
<td>Frequency Division Multiple Access</td>
</tr>
<tr>
<td>FEM</td>
<td>Finite Element Method</td>
</tr>
<tr>
<td>FR4</td>
<td>Flame Retardant 4</td>
</tr>
<tr>
<td>GbE</td>
<td>Gigabit Ethernet</td>
</tr>
<tr>
<td>HMSIW</td>
<td>Half-mode Substrate Integrated Waveguide</td>
</tr>
<tr>
<td>ISI</td>
<td>Inter-symbol Interference</td>
</tr>
<tr>
<td>LO</td>
<td>Local Oscillator</td>
</tr>
<tr>
<td>LVDS</td>
<td>Low-Voltage Differential Scheme</td>
</tr>
<tr>
<td>MCM</td>
<td>Multi-Chip Module</td>
</tr>
<tr>
<td>NIC</td>
<td>Negative Impedance Converter</td>
</tr>
<tr>
<td>Term</td>
<td>Definition</td>
</tr>
<tr>
<td>--------</td>
<td>-------------------------------------------------</td>
</tr>
<tr>
<td>NRZ</td>
<td>Nonreturn-to-Zero</td>
</tr>
<tr>
<td>QPSK</td>
<td>Quadrature Phase Shift Keying</td>
</tr>
<tr>
<td>PCB</td>
<td>Printed Circuit Board</td>
</tr>
<tr>
<td>PPW</td>
<td>Parallel-Plate Waveguide</td>
</tr>
<tr>
<td>p.u.l.</td>
<td>Per-Unit-Length</td>
</tr>
<tr>
<td>RF</td>
<td>Radio Frequency</td>
</tr>
<tr>
<td>RZ</td>
<td>Return-to-Zero</td>
</tr>
<tr>
<td>SERDES</td>
<td>Serializer De-serializer</td>
</tr>
<tr>
<td>SDR</td>
<td>Software Defined Radio</td>
</tr>
<tr>
<td>SiP</td>
<td>System-in-Package</td>
</tr>
<tr>
<td>SIW</td>
<td>Substrate Integrated Waveguide</td>
</tr>
<tr>
<td>SMA</td>
<td>SubMiniature version A</td>
</tr>
<tr>
<td>SNR</td>
<td>Signal-to-Noise Ratio</td>
</tr>
<tr>
<td>SoC</td>
<td>System-on-Chip</td>
</tr>
<tr>
<td>SOLT</td>
<td>Short-Open-Load-Thru</td>
</tr>
<tr>
<td>SoP</td>
<td>System-on-Package</td>
</tr>
<tr>
<td>TE</td>
<td>Transverse Electric</td>
</tr>
<tr>
<td>TEM</td>
<td>Transverse Electromagnetic</td>
</tr>
<tr>
<td>TM</td>
<td>Transverse Magnetic</td>
</tr>
<tr>
<td>VNA</td>
<td>Vector Network Analyzer</td>
</tr>
<tr>
<td>XAUI</td>
<td>10 Gigabit Attachment Unit Interface</td>
</tr>
</tbody>
</table>
Chapter 1

Introduction

1.1 Background and Motivation

Over the years, the semiconductor industry has been aggressively scaling down the minimum feature sizes of transistors and interconnects in order to improve the performance of modern electronic systems. As a result, cost, form factor and power consumption have come down significantly. This trend has tremendously increased the performance of digital circuits such as microprocessor and memory. Nonetheless, transistor scaling cannot solely provide and ensure the sophisticated agile operation needed in emerging applications, e.g., in wireless and biomedical domains, thus, further system integration and scaling are strived for. This fact has been acknowledged by the International Technology Roadmap for Semiconductors (ITRS) since 2005 [1]. As depicted in Fig. 1.1, the roadmap advocates the development and integration of several functionalities in conjunction with the core CMOS technology in order to continue the improvement of performance, and reduction of cost and power consumption. By using advanced circuit integration and packaging techniques, such as system-on-chip (SoC) [9], system-in-package (SiP) [10] and system-on-package (SoP) [11,12], it is expected that high-performance, multi-functional electronic systems populate the consumer market in a near future.

To meet the increasing demands for data processing required by many high-end applications, such as servers, storage devices and telecommunication networking equipments, there is a need to process or exchange information faster and faster. One of the metrics determining the processing capability of a chip is its clock frequency, which can be used to directly calculate the number of instructions that can be performed in a given time.
Introduction

Therefore, to achieve higher data throughput, higher clock frequency is often required. The ITRS has continually projected a growth in the local clock frequency, which is predicted to rise from a few gigahertz to 20 GHz by 2012, as seen in Table 1.1. In system operation, this means routing of ultra-high-speed data among a number of chips. As a result, the throughput is often limited by the bandwidth of off-chip interconnects. This is acknowledged by ITRS as labeled by “Off-Chip Speed” in Table 1.1. Although these numbers have been revised downward in the 2007 ITRS roadmap, it does not change the fact there is an increasing disparity between the CPU and off-chip bandwidths [13]. With the growth in utilizing multiprocessor core architectures, an aggregate off-chip bandwidth of 1 Tb/s may be needed in a near future [14]. Therefore, in the long term view of ITRS, novel interconnect solutions are required to provide satisfactory performance improvement of electronic systems.

![Fig. 1.1 Trend in the integration of multi-functional systems (adapted from [1]).](image)

<table>
<thead>
<tr>
<th>Year of Production</th>
<th>2005</th>
<th>2008</th>
<th>2010</th>
<th>2012</th>
</tr>
</thead>
<tbody>
<tr>
<td>On-Chip Local Clock (GHz)</td>
<td>5.204</td>
<td>10.972</td>
<td>15.079</td>
<td>20.065</td>
</tr>
<tr>
<td>Off-Chip Speed (GHz)</td>
<td>3.125</td>
<td>6.103</td>
<td>9.536</td>
<td>14.900</td>
</tr>
</tbody>
</table>
1.1 Background and Motivation

The rest of this section presents an overview of the challenges and solutions to achieve high-speed data communications. Specifically, the performance bottleneck of on- and off-chip interconnects are discussed in Section 1.1.1. A new trend in high-speed link architecture is described in Section 1.1.2. A comparison between electrical and optical solutions is briefly discussed in Section 1.1.3. Section 1.1.4 introduces some common high-speed approaches, and discusses the needs for alternative solutions.

1.1.1 Performance Bottleneck: Traditional Electrical Interconnects

While computing power is further enhanced by scaling the size of transistors, on-chip RC interconnect delay, which exceeds that of transistors, has been the main reason limiting the processing speed. Improved conductivity, new porous low-k dielectrics and interconnect scaling are currently employed to alleviate the delay problem [1]. On the other hand, introduction of new materials and processes has created reliability, integration and characterization challenges. For off-chip communications, chip-to-chip and backplane interconnects are the major obstacle limiting high-speed data transmissions. One of the main reasons behind this is that the low cost materials commonly used for these types of interconnects exhibit higher conductor and dielectric losses at high frequencies. Signal integrity of high-speed electronic systems is further degraded by the presence of discontinuities, such as vias, which add undesired parasitic effects that become significant at higher frequencies. In addition, highly integrated systems lead to more compact interconnect routing networks. The unwanted crosstalk and electromagnetic interference (EMI) are much more pronounced in applications with faster rise/fall times and data rates, and, thus, potentially lead to detection errors if not carefully avoided [15, 16]. Therefore, crosstalk and electromagnetic interference are the other major signal integrity concerns in designing compact systems containing highly integrated interconnect networks regardless of being on- or off-chips.

1.1.2 Need for High-Speed Serial I/O Architecture

To enable high-speed off-chip communications, serial links have become common high-speed input/output (I/O) architectures replacing their parallel counterparts (see Fig. 1.2) [17]. Generally speaking, in a parallel architecture, several hundred buses are required to achieve gigabit data rates. However, controlling crosstalk and synchronizing these many data lines to achieve high-speed transmission are extremely difficult [18]. This, in turns, limits
maximum achievable data rates. Moreover, this parallel solution requires a large number of I/O connections, and takes up more routing space. Parallel high-speed links also consume more power compared to serial links due to the multiplicity of the active and passive components. On the contrary, in the point-to-point serial architecture, several parallel data lines are multiplexed by a serializer and transmitted on a single link, as shown in Fig. 1.2. At the receiving end, a deserializer de-multiplexes the high-speed signal into its original parallel form. This approach significantly reduces a number of required interconnections, and the skew problem is drastically reduced. However, it results in more latency due to serialization and deserialization. A summary of the comparison between parallel and serial links is presented in Table 1.2. Considering the prevalence of serial signaling in many applications, the need for high-speed serial links is becoming increasingly prominent. The limited transmission bandwidth of the commonly used serial links is an artifact of the type of material and interconnect used for signaling. Therefore, research efforts have been directed towards exploring alternative interconnect structures such as optical interconnects.

![Fig. 1.2 I/O architectures.](image)

<table>
<thead>
<tr>
<th>Table 1.2</th>
<th>Comparison of Serial and Parallel Architectures</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Parameters</strong></td>
<td>Serial</td>
</tr>
<tr>
<td>I/O Pin Count</td>
<td>low</td>
</tr>
<tr>
<td>PCB Area</td>
<td>smaller</td>
</tr>
<tr>
<td>Power Dissipation</td>
<td>smaller</td>
</tr>
<tr>
<td>Timing Skew</td>
<td>smaller</td>
</tr>
<tr>
<td>Latency</td>
<td>larger</td>
</tr>
</tbody>
</table>
1.1.3 Electrical Vs. Optical Solutions

Optical interconnect technology is a promising approach to accommodate the increasing demands for high-speed data communication, as it provides very wide bandwidth with extremely low transmission loss. Optical fiber communication is now a standard method for delivering tens of gigabit data rates in long-haul communications and local-area networks (distances greater than 100 m). For the same reasons, optical interconnects are moving rapidly into rack-to-rack applications when the distances are greater than a few meters, as they are more favorable than conventional coaxial cables in terms of bandwidth, density and weight [19]. This technology is, however, not commercially viable for shorter distances (< 1 m), i.e., on-chip, on-package and on-board. The main limiting factors are cost, power consumption, performance of electro-optical devices and integration with existing electrical packages and systems [20].

Many studies have made a case that optical interconnects will outperform their electrical counterparts at the board and even chip levels, see [13, 21–23] for example. These investigations have based their conclusions more or less on a combination of these factors—bandwidth, density and length of the interconnect itself. A more inclusive work takes into account of the power consumption issues and the overhead engineering work in designing the driver and receiver needed in optoelectronic stages [23]. Nonetheless, one thing is clear that distance is the major determining factor for the viability of optical interconnect solutions. It is still uncertain that on-chip optical interconnects will offer an economical solution.

According to ITRS, on-chip electrical wires are still projected to provide the high-speed performance needed in future high-density electronic systems [1]. From the cost and complexity point of view, it is evident that electrical interconnects will play a major role at the package and board levels in delivering high-speed data transmission in a near-term future [19]. Nonetheless, alternative substrate materials and electrical-domain solutions are required to meet the demands of future high-speed communication systems. An electrical waveguide interconnect solution is, in fact, very well positioned for this challenge since it provides very low transmission losses and ultra-wide bandwidth. Furthermore, the interconnect can be easily integrated with the existing architectures without changing the signal domain.
1.1.4 Enabling Ultra-High-Speed Transmission Through Electrical-Domain Solutions

Few commercial serial I/O architectures used in backplanes can handle relatively high data rates, e.g., 3.125 Gb/s in XAUI (10 Gigabit Attachment Unit Interface) standard [18], provided that wide interconnect bandwidth is available. Common system hardware architectures may be able to support this bandwidth but often their interconnects are pushed to the limits especially when low cost lossy materials, such as FR4 that is commonly used in board fabrication. The next generation of wireline standard, 100GbE (100 Gigabit Ethernet), is expected to handle data rates up to 40 Gb/s on backplanes and even up to 100 Gb/s when interfacing with longer range fiber optic communication lines [24].

FR4-based materials are commonly used in fabrication of printed circuit boards (PCBs) and backplanes. The frequency-dependent losses in this type of substrate make digital baseband transmission even more susceptible to inter-symbol interference (ISI) when dealing with tens of gigabit data rate. this problem becomes more prominent in long interconnects. For instance, in a typical backplane, stripline interconnects are mostly used, which can be as long as half-meter or more. Fig. 1.3 shows simulated insertion loss of different interconnects (0.5 m in length) using Ansoft HFSS, a finite element electromagnetic solver [25]. It can be observed from the figure that high-frequency contents traveling through an FR4 stripline interconnect suffer drastic attenuation, which can be mainly attributed to the lossy dielectric. In contrast, low-loss laminates, such as Rogers RO4003C and RT/Duroid 5880, offer a much better transmission characteristic, especially at high frequencies, but at a higher cost than FR4 (see Fig. 1.3).

Alternatively, to achieve high-speed data communications over long lossy interconnects, several different techniques, such as differential signaling [17], equalization [26], multilevel signaling [27], are usually employed. Differential signaling is effective at reducing the effects of common-mode noise and increasing noise margin. An equalization scheme pre-emphasizes the high-frequency content of the transmitted signal to compensate for the channel attenuation profile. In a multilevel signaling approach, the baseband binary signal is re-coded to reduce the effective signal bandwidth; hence, distortion in the high-frequency region is alleviated [26,28]. These methods also come at a cost of more than doubling power consumption and increased complexity of the system.

It can be concluded that cheap and inherently lossy dielectric materials cannot sustain
future developments of high-speed systems, i.e., 40-Gb/s link and beyond. Electrical interconnects with low-loss substrate materials can still significantly improve the transmission quality over a long backplane to cope with the demand for higher data throughput while utilizing a similar system architecture [29]. Nonetheless, changing the substrate material alone will not achieve confined and efficient signaling in modern compact electronic systems, as crosstalk and EMI are a growing system design problem. Consequently, alternative interconnect structures and signaling techniques are needed to enable ultra-high-speed/high-frequency applications while maintaining signal integrity and minimal electromagnetic interference.

1.2 Thesis Contributions

In this thesis, an electrical waveguide-based interconnect is proposed to realize an all electrical-domain solution enabling the next generation high-speed data transmission systems. This is a low cost implementation as opposed to optical interconnects that have expensive fabrication and installation due to domain conversion and challenges in component alignment. In comparison with conventional lowpass planar interconnects, the wideband and low-loss advantages of a waveguide-based interconnect can be observed from transmis-
In this thesis, the effectiveness of the proposed method is proven, and the important aspects of design, optimization and characterization are presented. Furthermore, the integration challenges in utilizing this interconnect in high-speed signaling applications are addressed. Methods for compensating the size of the waveguide interconnects are also introduced. The research work utilizes both simulations and experiments in design and validation of the proposed approaches. Detailed thesis contributions are described below.

**Systematic design of the waveguide interconnect:** A two-dimensional (2-D) array of metallized via holes in a substrate material can be considered as an electromagnetic bandgap (EBG) substrate. It can be visualized that a waveguide can be formed in this substrate by creating a line defect in the periodic array, *i.e.*, removing rows of these via holes. This thesis proposes a systematic design of the waveguide by using the EBG concept to optimize the size of the vias and their spacing, and, ultimately, to provide a stopband in an ultra-wide frequency range. The method is also applicable to via structures that are nonuniform in the vertical direction. Furthermore, the optimization has demonstrated that only a single row of via fence is needed for each sidewall to efficiently provide signal propagation with negligible leakages. Hence, the new design approach enables waveguide-based interconnect structures that exhibit negligible leakages. This is very important in designing practical routing structures such as bends. Excellent isolation property is demonstrated by presenting the performance characteristics of several bend geometries. In addition, a via-fence structure is proposed in a multiple waveguide geometry in order to reduce crosstalk between the coplanar transitions. The performance of the waveguide interconnect is also evaluated from a signal integrity perspective, which include crosstalk, losses and timing performance. This work produced two conference proceeding papers [C.8, C.10] and one journal article [J.4].

**System integration for high-speed digital transmission:** The two main challenges in utilizing a waveguide interconnect for high-speed digital signaling have been addressed in this thesis. Due to the three-dimensional nature of the waveguide and its incompatibility with planar structures, adaptors and transitions are needed. The design of the coplanar, via and aperture transitions is investigated in which important design parameters are identified. Fullwave parametric simulations are employed to study the importance of the geometrical parameters in the design and optimization of each transition. New circuit models are proposed for the via and aperture transition structures. These
1.2 Thesis Contributions

models offer capabilities for circuit-based simulations and fast turn-around time in design and optimization of these transition sections. To examine the validity range of each model, error analysis in comparison with fullwave simulations is also performed. Measurements of fabricated prototypes containing the studied transition sections confirmed the accuracy of the models.

The second system integration challenge arises due to the bandpass characteristic of the waveguide. Baseband signals cannot be transmitted directly through a bandpass channel. In this work, modifying the driver and receiver blocks of the conventional high-speed systems is proposed. These blocks instead of being simple amplifiers include up-conversion and down-conversion mixers. This modification is, in fact, adding modulation and demodulation in signal transmission process. This is the first time that such a system has been developed using electrical waveguide interconnects. The performance of the proposed system is evaluated by simulations through timing analysis. As a result, two conference proceeding papers [C.8–C.9] and one journal article [J.3] were published.

**System implementation for high-speed digital transmission:** To validate the proposed high-speed system, the first experimental evaluation of the waveguide-based interconnect system has been demonstrated at the data rate of 2.5 Gb/s. Subsequently, the developed system is re-designed and improved to illustrate excellent transmission quality up to maximum data rate of 5 Gb/s. Several prototypes were fabricated using FR4, ceramic and Rogers™ materials. One conference proceeding paper [C.6] and one journal article [J.2] reported these contributions. A provisional patent [P.1] was also filed for this invention and the subsequent contributions.

**Introducing new hybrid waveguide structures to enable ultra-high-speed transmission:** To overcome the relatively large footprint of the waveguide, a new routing method is proposed by inserting one or more lowpass interconnects inside the waveguide. This technique creates a hybrid structure with increased channel capacity by simultaneously utilizing the lowpass and bandpass channels. The engineering challenges in this structure include maintaining signal integrity by ensuring minimal change in the characteristic impedance of the embedded striplines and crosstalk. Such issues are investigated in this thesis. Efficient transition is also proposed for routing striplines in and out of the waveguide. Maximum aggregate transmission rate of 15 Gb/s with excellent output eye quality has been achieved experimentally for a hybrid waveguide structure containing two embedded striplines, which demonstrates the feasibility of ultra-high-speed transmissions.
Two conference proceeding papers [C.1–C.2] and one journal article [J.2] were published from this work. One conference paper also received the Intel best student paper award at the 16th IEEE Electrical Performance of Electronic Packaging conference, and the other paper was selected as a finalist to take part in the student paper competition at the Antennas and Propagation symposium.

**Enabling parallel channel transmission by using waveguide interconnect:** Another approach to increase the waveguide channel capacity is proposed by using the multimode transmission concept. As opposed to the hybrid approach, which physically adds additional interconnect structures, different orthogonal modes are harnessed for parallel signaling through the same physical channel. An efficient transition structure for exciting the TE\textsubscript{20} mode is proposed in this thesis. In addition, a multimode double launcher is proposed in order to provide simultaneous transmission of the TE\textsubscript{10} and TE\textsubscript{20} channels along the shared waveguide medium. A waveguide-based balun is also introduced to provide a truly balanced structure required to efficiently generate the needed differential-mode input at the coplanar TE\textsubscript{20} transition. Several prototypes were fabricated to validate the concept experimentally through frequency-domain measurements. Furthermore, a high-speed band-pass system is implemented to demonstrate excellent dual-channel transmission through the developed multimode structure at the data rate of 1 Gb/s. Overall, the proposed technique is proved to be an effective method of creating two communication channels in the same waveguide interconnect. One journal article [J.1] was produced as a result of this work.

### 1.3 Publications

**Refereed Journal Papers:**


1.3 Publications


Conference Proceeding Papers/Presentations:


1.4 Outline of the Thesis

The rest of the thesis is outlined and organized as the following. Chapter 2 presents an overview of some signaling techniques and electrical interconnect structures reported in the chip-, package- or board-level systems. The common goal of these approaches is to handle higher communication throughput between devices. They are the state-of-the-art technologies utilizing electrical-domain solutions as opposed to the costly optical counterparts.

In Chapter 3, a systematic approach based on the EBG concept for designing the waveguide interconnect is described. Subsequently, its transmission performance is compared with common planar transmission lines in order to determine the advantages of this alternative routing method. In addition, optimization of the design of a number of bend structures is presented followed by fullwave investigations. Furthermore, the crosstalk levels at the near-end and the far-end of multiple interconnects are investigated. Multiple microstrip lines are used as the benchmark for evaluating the studied interconnects. In addition, a via fence structure is proposed to be incorporated in the transition sections of multiple interconnects in order to improve the crosstalk immunity.
Two transition structures, \textit{i.e.}, via and aperture transitions, for 3-D integration of the waveguide interconnects are investigated in Chapter 4. The design of these transitions using parametric fullwave simulations is presented. The general modeling approach to extract the equivalent circuits of these two structures is also described. A finite element method (FEM) solver is used to validate the circuit models. Furthermore, error analysis is also employed to examine the sensitivity of the models to variations of geometrical parameters and frequency of operation. As well, two waveguide prototypes containing the studied transition structures are fabricated, and the proposed transition models are validated with measured results.

Chapter 5 describes the implementation of the waveguide interconnect system for high-speed digital transmission. The specifics of the components needed for baseband signal transmission using substrate integrated waveguides are detailed and discussed. Fabricated waveguide prototype is characterized in frequency domain to demonstrate its operating bandwidth. The operation of the single channel waveguide system at 3.125 Gb/s and 5 Gb/s is demonstrated experimentally.

In Chapter 6, a method for reusing physical waveguide channel is proposed to achieve ultra-high-speed transmission. The technique presents a hybrid approach in which simultaneous transmission occurs in both waveguide and embedded stripline channels. Hybrid structures and the needed transition geometry for routing the striplines in and out of the waveguide are proposed and evaluated using fullwave simulations. Measurements of fabricated hybrid prototypes demonstrate achieving maximum aggregate transmission rate of 15 Gb/s. Subsequently, a comparative study using system simulations is presented to illustrate the ultra-high-speed channel capacity of the proposed waveguide-based approach when wideband system components are incorporated.

An alternative approach for achieving multichannel data transmission is proposed and investigated in Chapter 7. By employing the multimode transmission concept, orthogonal waveguide modes, specifically TE$_{10}$ and TE$_{20}$, are used to create parallel channels inside the same waveguide medium without adding physical transmission lines. To excite these two orthogonal modes simultaneously, a multimode double launcher is introduced and characterized. Furthermore, a balun structure based on a substrate integrated waveguide is presented and included in the multimode waveguide in order to efficiently excite the TE$_{20}$ mode. A number of fabricated waveguide prototypes are experimentally characterized to validate the proposed concept. In addition, a high-speed bandpass system is implemented...
to demonstrate parallel dual-channel signaling.

Finally, the research work is summarized in Chapter 8, followed by projection of the future research works in this field.
Chapter 2

Signaling Techniques and High-Speed Interconnect Technologies

2.1 Introduction

An interconnect has the role of guiding clock or data to a target destination or to provide power and ground connections of an electronic system. The performance of interconnects has become a critical design factor in many high-end systems demanding high-speed data transmission. At the chip level, the continuation of transistor scaling has reduced device transition delays, especially in logic gates, leaving on-chip interconnect delay as the dominant factor [30]. Due to the miniaturization trend, conductor line width has reduced resulting in increased per-unit-length (p.u.l.) resistance, and, thus, the RC delay. Large latency brings inefficiency to the information processing, as several clock cycles are wasted without any actions. In addition, a skew between clock and data lines may be increased creating synchronization problems. This has not been a major issue for local interconnects, which connect closely grouped transistors, since their length is also scaled down, but global interconnects that provide connectivity between large modules and the input/output circuitries across a chip display a different scaling behavior [1,31]. In fact, the length of global interconnects remains almost unchanged between technology nodes, which continue to impose a major communication bottleneck between many high-speed on-chip circuitries [32].

Over the past years, an exploration of new composite materials with lower resistivity or low-k dielectrics has been started, which is projected to be an effective solution, particularly,
for local wires in a near future [1]. In fact, improving copper resistivity has been more successful than employing low-K materials, as they are porous, and impose many integration challenges using existing fabrication methods [1]. Nonetheless, the 2005 ITRS roadmap still calls for efforts in the reduction of dielectric constant by developing new porous low-k dielectrics, based on silicas or organic polymers, and hybrid dielectric stacks with airgap architecture [1]. As for the long-term challenge, it is predicted that innovative materials will not suffice to meet the performance requirements for global on-chip interconnects of the future generations of high-speed systems [1]. The roadmap has suggested introduction of novel interconnects as the alternative solution, which include optical interconnects, RF interconnects or vertical integration techniques. The common goal is to reduce delay and power consumption, and improve and bandwidth of the interconnects.

Chip-to-chip communications, which provide longer connectivity (compared to on-chip links) at the substrate and board levels, present another challenge in high-speed communications. As mentioned in the previous chapter, dielectric loss and discontinuities are critical factors limiting the interconnect performance in the high-frequency regime. In this chapter, different state-of-the-art techniques for improving transmission quality for intra- and inter-chip communications are reviewed. Some traditional signaling methods for achieving high-speed data transmissions between chips are discussed in Section 2.2. Section 2.3 describes pulse shaping techniques, which aim at adapting the transmitted signal to the interconnect channel characteristics. In Section 2.4, novel interconnect structures enabling high-speed signaling are presented.

2.2 Signaling Techniques

2.2.1 Parallel Systems

As mentioned in Chapter 1, serial links are employed in high-speed signaling as they offer area and power savings. The latency of the overhead circuitries is not significant when the overall delay is dominated by long interconnects. The latency due to serializer and deserializer becomes critical for systems, such as multiprocessor networks and CPU-memory links, where the interconnect delay is much smaller [33]. In these situations, parallel links are typically employed to reduce latency. An example of multi-gigabit parallel interfaces is Rambus Redwood interface, which can achieve up to 6.4 Gb/s/channel (typically 8 or 16
lanes per chip) of data rates with an equalization technique [34].

2.2.2 Multilevel Signaling

Multilevel coding is used to compress the signal bandwidth by encoding several bits over the same symbol period. Using this technique, vulnerability to high-frequency losses is reduced, and the transmitted bit rate is increased. Due to its relative ease of implementation, pulse amplitude modulation (PAM), particularly 4-PAM, is generally employed, which requires DAC for the transmitter and ADC for the receiver [33]. In [26, 27], 4-PAM, which maps every two bits of data into one of the four possible signal levels, is used in conjunction with an equalization technique to enhance the data rate and quality of transmission up to 8 Gb/s. Duobinary signaling is another multilevel coding scheme that is being investigated as an alternative to 4-PAM [28]. A duobinary code [35], as illustrated in Fig 2.1, is formed by adding two successive pulses to yield the output [2]

\[ y_k = a_k + a_{k-1}. \] (2.1)

The advantages of using duobinary technique over 4-PAM are larger SNR, less power and less circuit complexity. By utilizing pre-emphasis and duobinary signaling, 10-Gb/s and 25-Gb/s signal transmissions with low bit error ratio (BER < 10^{-13}) through 35-cm and longer FR4-based backplane interconnects were reported [28, 36]. Multilevel signaling approach can be applied to any type of interconnects in order to further enhance the channel capacity.

\[ \{a_k\} \]

\[ \{y_k\} \]

\[ \text{Delay } T \]

Fig. 2.1 Duobinary signaling [2].
2.3 Pulse Shaping

2.3.1 Near-Speed-of-Light Signaling

Traditionally, repeaters are used to periodically re-shape transmitted pulses along global on-chip interconnects in order to improve the system delay. Due to finite gain and parasitic capacitances of the repeater circuits, a repeater also adds delay to the system [37]. Increasing the number of repeaters improves the rise time of the pulse. However, this technique further complicates the routing and floor planning, and comes at the expense of more power and area consumption.

On-chip interconnects behave like a transmission line at high frequencies in which simple RC elements can no longer be used for modeling. Essentially, the phase velocity of the signal traveling on the interconnects is proportional to $1/\sqrt{LC}$ instead of $\sqrt{\omega/RC}$, as illustrated in Fig. 2.2. These relationships can be derived by considering the transmission line model shown in Fig. 2.3, which represents a small segment of an interconnect. $R$, $L$, $G$, and $C$ are p.u.l. quantities.

![Fig. 2.2](image)

**Fig. 2.2** Normalized phase velocity of minimum-sized on-chip interconnects and frequency spectrum of a trapezoidal pulse [3]. The phase velocity is normalized to the speed of light in silicon dioxide.

The telegrapher’s equations can be found from this model, and, subsequently, the propagation is derived as [38]:

$$\gamma = \alpha + j\beta = \sqrt{(R + j\omega L)(G + j\omega C)}. \quad (2.2)$$
α and β are attenuation and phase constants, respectively. Assuming negligible conductance and at low frequencies \((R \gg \omega L)\), the propagation constant in (2.2) is simplified to:

\[
\gamma = \sqrt{j\omega RC} = \sqrt{\omega RC \left( \frac{1}{\sqrt{2}} + \frac{j}{\sqrt{2}} \right)}.
\]  

(2.3)

Hence, the phase velocity \((v_p)\) in the RC dominated region is expressed as:

\[
v_p = \frac{\omega}{\beta} = \sqrt{\frac{2\omega}{RC}}.
\]  

(2.4)

At higher frequencies where \(R \ll \omega L\) and \(G \ll \omega C\), the propagation constant can be approximated to:

\[
\gamma = j\omega \sqrt{LC} \left( 1 + \frac{R}{2j\omega L} \right) \left( 1 + \frac{G}{2j\omega C} \right)^{1/2} \approx j\omega \sqrt{LC} \left( 1 + \frac{R}{2j\omega L} \right) \left( 1 + \frac{G}{2j\omega C} \right) \quad (2.5a)
\]

\[
\approx j\omega \sqrt{LC} \left[ 1 + \frac{1}{2j\omega} \left( \frac{R}{L} + \frac{G}{C} \right) - \frac{RG}{4\omega^2 LC} \right].
\]  

(2.5b)

\[
\gamma = j\omega \sqrt{LC} \left[ 1 + \frac{1}{2j\omega} \left( \frac{R}{L} + \frac{G}{C} \right) - \frac{RG}{4\omega^2 LC} \right].
\]  

(2.5c)

Since the last term on the right hand side of (2.5c) can be neglected at high frequencies, the phase constant and phase velocity are found to be:

\[
\beta \approx \omega \sqrt{LC}.
\]  

(2.6a)

\[
v_p \approx \frac{1}{\sqrt{LC}}.
\]  

(2.6b)
This implies that the high-frequency contents of the signal can travel near the speed of light. Typically, in a digital nonreturn-to-zero (NRZ) pulse, most of its energy is concentrated in the lower part of the signal spectrum, \( i.e., 1/T_b \) Hz (\( T_b = \) bit width). For this reason, these baseband signals experience greater delays when traveling through on-chip interconnects compared to off-chip, which have wider cross-sectional width and, hence, behave similar to the high-frequency case.

This idea was exploited in [3, 37]; the spectrum of a baseband signal is shifted to a higher frequency band by modulation to operate with near-speed-of-light (at the dielectric) velocity and reduce wire latency. However, due to the lowpass nature of these interconnects, the modulated pulse will experience higher attenuation. In practical implementation, the LC regime can be achieved at a relatively low frequency region by properly choosing the interconnect dimensions. For example, a wider interconnect has less p.u.l. resistance and its inductive effect becomes prominent at lower frequencies. In [3], a microstrip line as opposed to a simple metal wire is chosen as an on-chip interconnect due to having a well-defined return path (easier to design for a desired inductance value). The performance of the transmitter and receiver must also be optimized in designing such a system, as not to introduce excessive delay and degradation. Higher inductance also increases the line impedance, which requires low-swing voltage and consumes less power. In [3], a baseband signal was directly modulated by a passive ring mixer at the driver. The receiver was implemented by using a double-balanced mixer. The system was demonstrated for the data rate of 2 Gb/s, which was modulated by a 7.5-GHz sinusoidal source consuming 16 mW of power. The total delay from the input to output of the test chip was measured to be 322 ps for the falling edge and 490 ps for the rising edge. The measured delay included the output inverter delay (123 ps), which was employed for measurement purpose. Ignoring the inverter, the proposed system had an average delay of 283 ps over a 20-mm long interconnect as opposed to 400 ps when repeaters are used (wide metal interconnects). Half the speed of light in silicon dioxide was achieved using this approach. Overall, this method employs a simple modulation scheme, \( i.e., \) BPSK (Binary Phase Shift Keying), to achieve delay improvement without consuming significant power. The drawback here is that still lowpass interconnects, which have limited bandwidth and are prone to crosstalk and EMI, are used as the transmission medium.
2.3 Pulse Shaping

2.3.2 Pulsed Current Mode Signaling

To avoid the large transistor sizes often employed in a voltage-mode driver, current-mode signaling is used to provide a high impedance driver [39–42] with reduced delay and power consumption in high-speed signaling. As discussed in Section 2.3.1, in lossy on-chip interconnects, near-speed-of-light velocity can be achieved at the high-frequency region. In the method described here, instead of modulating the pulse, return-to-zero (RZ) signaling is utilized as a simpler technique for shifting the frequency content of the baseband signal towards the LC region. As opposed to the NRZ scheme, as shown in Fig. 2.4, an RZ pulse occupies a fraction of the bit width, i.e., the bandwidth of an RZ signal is concentrated at higher frequency region than that of an NRZ signal. By optimizing the pulse width of an RZ bit, ISI effect can also be alleviated due to an extra time interval before the next bit.

![Fig. 2.4](image)

Fig. 2.4  Polar NRZ and RZ binary formats with their respective normalized power spectrum density (PSD) [4].

With the differential current-mode RZ signaling, 8-Gb/s data transmission with BER of less than $10^{-14}$ was demonstrated over a 3-mm long on-chip CPW interconnect using the 0.18-μm CMOS technology [42]. The link latency of 19.4 ps was achieved compared to a link with conventional repeaters of 55 ps. The power consumption of the current-mode driver with output multiplexing (0.29 pJ/bit) was very small in comparison with that of a conventional link (0.7 pJ/bit). However, significant power (3.1 pJ/bit) was dissipated through the overhead circuitries, such as delay locked loops (DLLs) and skewing and de-
skewing latches. It was suggested that the system design could be scaled to provide the maximum data rate of 16 Gb/s and drive a link of up to 8-mm long at the expense of increased power consumption. It is speculated that transmission over a longer link could also be achieved with reducing line attenuation by using the concept of distributed loss compensation [42]. This was demonstrated by using a distributed amplifier in place of conventional repeaters over a 14-mm long CPW for 3-Gb/s data transmission with BER less than $10^{-14}$. The method is similar to low-voltage differential scheme (LVDS). The drawback is the increased latency. Significant power saving is the advantage of this approach (2 pJ/bit v.s. 7 pJ/bit for an identical link using a conventional repeater technique).

2.3.3 Equalization

In communication systems, intersymbol interference (ISI) is a phenomenon describing interferences between bits in a pulse sequence, which results from suboptimum filtering occurring in the channel [43]. Conventional transmission lines impose such filtering characteristics due to higher attenuation as frequency increases. High-speed digital pulses, which are broadband in nature, in transmission through these channels, experience attenuation as well as slower rise and fall times. Together with other signal integrity issues, such as electromagnetic coupling, dispersion, reflections from circuit terminations, package and connector discontinuities, ISI is one of the main sources of error in high-speed communications. To combat ISI and dispersion, equalization techniques are used to compensate for the disparity between the low- and high-frequency characteristics of the channel. As depicted in Fig. 2.5, a transmitter equalizer whose transfer function conceptually produces an inverted channel response (inverse of interconnect response with accentuated highpass characteristic) is added in the transmitter section. This renders an overall flat response for the system. In practical implementation, it is easier to attenuate the low-frequency components than amplifying the high-frequency contents, however, this comes at the expense of lower SNR. This approach is referred to as pre-equalization, which was first demonstrated in [44] for a 4-Gb/s serial channel. Finite impulse response (FIR) filters compatible with standard CMOS processes are commonly used for the implementation of pre-emphasis filters. Other pre-emphasis transmitters were also demonstrated for high-speed serial communications in [45,46] to achieve up to 10-Gb/s data rate over a 10-m long copper coaxial cable (with multilevel coding).
An equalizer can also be implemented in the receiver section, which is referred to as receiver equalization. Typically, a combination of ADC followed by digital filters, which are more flexible and easier to implement than their analog counterparts, is a more common architecture, which is reported to have achieved a maximum data rate around 8 Gb/s [47]. An example of high-speed link implementation using the receiver equalization approach was presented in [48]. Equalization can be made adaptive corresponding to the channel response. As opposed to transmitter equalizer, the channel characteristic is not required in the receiver equalization scheme. The drawback is that the high-frequency noise is also amplified in the process. As well, more complicated circuitries, e.g., high-performance ADCs are needed that are harder to implement compared to high-speed DACs [33]. However, DACs are much more sensitive to clock jitter, which is the dominant performance limiter. Another method worth mentioning here is decision-feedback equalizations, which corrects the ISI based on the previous decision of the detected symbol. Due to the latency of the feedback loop, the method is limited to a few Gb/s of transmission rate [47]. In addition, it also suffers from error propagation. Generally, equalization is adopted both at the transmitter and receiver sides to achieve a reliable high-speed link over a long FR4 backplane (up to 6.4 Gb/s) [49]. Nonetheless, the equalization techniques come at the cost of increased complexity and power consumption.

2.4 New Interconnects

2.4.1 Wireless Interconnects

Global on-chip interconnect delay problem mentioned earlier not only affects signal lines but also global clock networks, which are used for system synchronization. A wireless inter-
connect is a technique that can deliver signals across a chip via transmitting and receiving antennas without any physical conductor transmission mediums. In fact, a wireless clock distribution system was proposed in order to deliver clock signals at the speed of light (in the dielectric) [5, 50]. This concept can be illustrated by the schematic in Fig. 2.6. The transmitter (Tx) broadcasts the clock signal in a single tone at microwave frequency, e.g., 15 GHz in [5] or higher, in order to limit the size of on-chip antennas. The received single-tone clock signal is eventually divided and re-shaped at Rx into the desired clock waveform. The receiving antennas are distributed on the chip, and the transmitting antenna is placed on the same die. It can be immediately observed that the potential obstacle to this approach is the relatively larger size of the antennas. Each antenna in [5] was as large as 0.6 × 2 mm², which can be too large for intra-chip communications. It can be speculated that the modulating frequency can be increased to reduce the antenna area, but the design and complexity of the circuits will increase and cost will be a concern. Nonetheless, the wireless clock distribution system is a very promising approach in inter-chip synchronization, for example, in an MCM system [51]. In this manner, the transmitting clock antenna can be located off-chip and acts as the reference frequency for the entire system. Another concern is that such a system is more sensitive to noise and EMI compared to those of guided-wave approaches.

![Fig. 2.6 An on-chip wireless clock distribution network using dipole antennas [5].](image)

### 2.4.2 Reconfigurable Interconnect System

As discussed in the preceding section, the wireless approach is viable for clock signals. However, it is not suitable for digital signal transmission, especially broadband or high-speed, as there is a limitation in the antenna bandwidth. An alternative method is proposed
2.4 New Interconnects

in [6, 52], which is based on capacitive coupling between on-chip drivers and receivers on a common microstrip or CPW transmission line, as shown in Fig. 2.7. The transmission line has a very low conductor loss due to the larger width (10–100 µm) compared to that of ULSI interconnects (0.1–1.0 µm). In the proposed system architecture, the low-loss interconnect was used as a shared transmission medium within and between chips on an MCM substrate. The drivers and receivers communicate via the shared transmission line by means of capacitive couplers, as depicted in Fig. 2.7. To differentiate between the communication channels, frequency division multiple access (FDMA) and/or code division multiple access (CDMA) techniques are used to link between appropriate driver and receiver pairs. Furthermore, these schemes minimize interferences between communication channels within the same transmission medium. The CDMA technique offers a lot of flexibility to the system in re-routing signal paths. In addition, FDMA can be employed in conjunction with the CDMA method to further increase the channel capacity of the system by creating more communication frequency bands. One of the drawbacks for this approach is that the power delivered to each receiver decreases as the number of I/O channels increases, and less signal power will affect the BER due to a reduced SNR. Current CMOS technology is not a very efficient platform for fabricating high-performance RF/microwave circuits such as multipliers and mixers. Therefore, maximum achievable data rates will be limited by the performance of the these components. Nonetheless, this scheme can potentially save routing space, as different on-chip signal lines can be multiplexed on the same channel. There are, however, other challenges in utilizing this approach such as the added latency and complexity due to the overhead electronics. Finally, this approach must be competitive in terms of cost, power and form factor to be considered as an alternative to current global interconnect and ball grid array (BGA) technologies [20].

2.4.3 AC Coupled Interconnects

Another type of emerging interconnect close to the geometry described in Section 2.4.2, however, in a point-to-point manner, is the AC coupled interconnect (ACCI) [7]. In this scheme, capacitive or inductive coupling is used as a mechanism in transferring information between IC and substrate or stacked ICs, as depicted in Fig. 2.8. High density I/Os between chips can be created by using these 3-D interconnects, which can be fabricated with existing CMOS processes. Nonetheless, wire bonds, micro bumps or through-silicon vias are still
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Fig. 2.7 A reconfigurable RF/wireless interconnect system with multiple I/Os [6].

needed for power and ground connections, which will all reduce the operation bandwidth.

A capacitive ACCI typically exhibits low power consumption. The required distance between the parallel plates is relatively small, on the order of a few microns [7]. This limits its usage to face-to-face stacking of ICs. Nonetheless, the capacitive ACCI has been employed in high-speed chip-to-chip communications on an MCM substrate [53]. The top capacitor plate is embedded on a chip whereas the lower section is in the substrate. The plate alignment is achieved by using solder bumps, which also provide DC power and ground connections. In [53], 2.5 Gb/s/channel transmission over 56-mm long microstrip was reported in the 0.35-µm CMOS technology. Bit error rate of less than $10^{-12}$ and peak-to-peak jitter below 120 ps were measured. Power consumption in the transmitter and receiver were 10.3 mW and 15 mW, respectively. The solder-bump technology is not compatible
with PCB laminates. In fact, in another literature report [54], wire bonds were used for interconnections between ACCI and PCB interconnects. The circuitries were implemented on the 0.18-$\mu$m CMOS technology, and 3-Gb/s transmission was demonstrated across 15-cm long microstrip line on an FR4 substrate. This type of I/O would also eliminate via stubs, which is one of the main sources of signal integrity degradation in high-speed signaling.

For low supply voltages, an inductive ACCI is preferred, as the capacitive coupling technique is a voltage-driven scheme [55]. The required distance between inductors to achieve sufficient coupling is on the order of tens of microns. Therefore, this interconnect scheme provides more flexibility in which the face-up or face-down stacked structure can be employed. In [55], 1.25-Gb/s/channel transmission between 60-$\mu$m spaced coupled inductors was demonstrated in the 0.35-$\mu$m CMOS technology with the total interface area of 0.025 mm$^2$. Power consumption in the transmitter and receiver were 43 mW and 2.6 mW, respectively. By using this approach, aggregate transmission rate of 195 Gb/s for 195 channels over 4 stacked chips was achieved using the 0.25-$\mu$m CMOS process in [56]. The total power consumption was 4.1 W. This approach is mostly suitable for ultra-short distance applications such as die-to-die connection. Crosstalk between the inductors and circuitries seems to have limited the data rate of each channel.

### 2.5 Summary

The performance of high-speed communications links is limited by the conductor and dielectric losses and parasitic effects from package discontinuities and connectors. Several electrical-domain techniques for enhancing the link performance, which are the preferred solutions due to low cost and their compatibility with existing systems, are discussed in this chapter. Parallel systems are mostly suitable for very-short-distance communication links, such as memory or logic-to-logic interfaces, which often require low latency and power consumption without adding a lot of overheads. In the serial schemes, interconnect delay is a major concern especially for on-chip links. Pulse shaping techniques, such as near-speed-of-light transmission and pulsed current mode signaling, were proposed to overcome this latency problem. Near-speed-of-light signaling is achieved by modulating baseband signals into the LC region of on-chip interconnects. Pulsed current mode signaling is motivated by the same principle; however, the modulation is avoided by utilizing RZ signaling. In off-chip communications where ISI due to the channel characteristic is more of a concern, equal-
ization and multilevel coding are often used together to extend the maximum transmission capacity. Alternatives to pulse shaping are novel interconnects that are also discussed in this chapter. Specifically, wireless interconnects provide speed-of-light transmission for wireless intra- or inter-chip clock distribution networks. AC-coupled interconnects avoid the effects of common package discontinuities by utilizing 3-D integration schemes. The AC coupled interconnects were also adapted to employ FDMA and CDMA techniques to provide a reconfigurable interconnect system.
Chapter 3

Design and Characterization of Waveguide Interconnects

3.1 Introduction

The waveguide interconnect is configured within the circuit substrate, and its sidewalls are formed by utilizing via fences. In order to provide a systematic way to minimize the sidewall leakage of the interconnect, the electromagnetic bandgap (EBG) concept is employed. In Section 3.3, a two-step design methodology is suggested, which starts by designing the EBG substrate followed by determining the waveguiding width that forms the interconnect in the EBG host medium. The design example of the basic through (single) interconnect is also included. In Section 3.4, the waveguide performance is compared with conventional planar transmission lines in order to determine the advantages of this alternative routing method. Optimization of the design is presented followed by fullwave investigation of a number of bend structures in Section 3.5. Furthermore, the near-end and the far-end crosstalk of multiple waveguide interconnects are investigated in Section 3.6. Multiple microstrip lines are used as the benchmark for evaluating the studied waveguides. Waveguide transitions are introduced in Section 3.7. Design of the coplanar microstrip-to-waveguide transition is also investigated in the same section. Finally, in Section 3.8, a via fence structure is proposed to be incorporated in the transition sections of multiple interconnects in order to improve the crosstalk immunity.
3.2 A Substrate Integrated Waveguide

Typically, waveguides offer a shielded transmission medium. In traditional sense, they are solid waveguides, which have a rectangular, circular or elliptical shape. These conventional waveguides are bulky; hence, they are not suitable for board-level integration. Recently, novel types of interconnects that are fully compatible with electrical systems are introduced. These interconnects are based on microwave waveguide structures that are now integrated into the electronic system substrate [57]. Examples of these synthesized waveguides are substrate integrated waveguide (SIW) [58] or electromagnetic bandgap (EBG) waveguide-based interconnect [59, 60] and substrate integrated non-radiated dielectric (SINRD) guide [58].

A substrate integrated waveguide interconnect is a rectangular waveguide configured within the circuit substrate, and its sidewalls are formed by utilizing rows of metallic via holes, as depicted in Fig. 3.1. This type of waveguide interconnect was first introduced in [61], and, subsequently, as laminate waveguide in [62, 63]. It has been utilized as a low cost microwave and millimeter-wave component developed by using PCB fabrication technologies [58]. The adaptation of waveguides to PCB technology along with its inherent low-loss bandpass characteristic has made them attractive structures for usage in analog and even for high-speed digital signaling [64] in highly integrated circuits. Nevertheless, many challenges still exist in integrating this type of non-planar interconnect with conventional electronic circuits especially in digital applications, as will be discussed in this thesis.

![Fig. 3.1 A substrate integrated waveguide.](image-url)
3.2.1 Integration Challenge: Analog and Digital Perspectives

Being a 3-D structure, a substrate integrated waveguide cannot be directly connected to traditional planar circuits. Therefore, several efficient transition sections have been investigated. A microstrip-to-waveguide coplanar transition was proposed in [65], and proved to be very efficient and wideband. In [63], a microstrip-to-waveguide via transition was used to excite the waveguide antenna array. An aperture transition that connects between two waveguides vertically was presented in [62,66], which will be elaborated along with the via transition in Chapter 4. The CPW-to-SIW transition that alleviates the substrate thickness limitation from the coplanar transition was introduced in [67]. Other variations of these transitions have also been reported in [68–72]. Once the appropriate transition sections are properly designed, the waveguide can be employed as an interconnect in analog and digital applications.

Many microwave and millimeter-wave passive devices have been implemented utilizing SIWs such as antennas [73–75], circulators [76], diplexers [77], filters [78–80], phase shifters [81], power dividers [82], and resonators [69,83,84]. Substrate integrated waveguides have also been incorporated in many analog sub-systems. For instance, the waveguide structure is integrated in a mixer circuit to provide extra isolation between LO and RF ports [85]. The waveguides have also been employed as antennas and filters, and they are demonstrated to be efficiently utilized in millimeter-wave front-end applications [86,87]. In another study, SIW power dividers and couplers were used as the building blocks for a six-port software-defined radio (SDR) receiver platform [88, 89]. In the receiver architecture of [89], the received RF signal is routed by utilizing a six-port SIW junction to power detectors.

In digital applications, in addition to the need for transition for system integration, the driver and receiver stages should be modified due to the bandpass characteristic of the waveguide. This will be discussed in detail in Section 5.3.

3.2.2 Miniaturization

The SIW interconnect is a bulky component with its width being the largest cross-sectional dimension. Its thickness can be as thin as the fabrication technology allows along with power handling considerations. The width of the substrate integrated waveguide is determined by the frequency range of operation and the dielectric constant of its filling material. The TE\(_{10}\) mode is the dominant transmission mode, and its cutoff frequency yields the
width of the waveguide. As this frequency increases, the waveguide becomes narrower. At
tens of gigahertz frequency range, the waveguide width is still relatively large compared to
that of a microstrip or stripline. This constraints employing waveguides in compact pack-
ing environments. A few approaches have been proposed to alleviate this issue. The size
reduction, as suggested in [90], can be achieved by folding the waveguide but this increases
its height [91]. The folded waveguide can be imagined as two SIWs stacked on top of each
other with a gap at one end of the common conductor plane.

Another method, which is proposed in [92], benefits from the symmetry of cross-sectional
electric field profile and removes half of the waveguide in longitudinal direction. This
creates half-mode propagation in the half waveguide, thus, called half-mode waveguide. The
magnetic wall is achieved by leaving one of the sidewalls open but it does not truly represent
a magnetic wall, as can be seen from fullwave simulations. Therefore, the interconnect is a
source of field emissions at the open wall while size reduction by almost 50% is achieved.

Another way to compensate the large footprint problem is by efficient use of the sub-
strate and increasing the channel capacity per volume. This method employs different
modes of transmission in the same space. Therefore, multiple communication channels are
created inside the same substrate volume. These solutions are presented in Chapters 6 and
7.

3.3 Design and Optimization

An EBG waveguide-based interconnect is the term used initially in this thesis to refer to
the signal guiding structure that is presented in Fig. 3.2, as the interconnect can be visu-
alized by removing rows of vias in a 2-D EBG substrate. The EBG structure is composed
of a dielectric layer sandwiched between two solid conductor planes that are electrically
connected by periodic metallized through via holes. When one or more rows of vias are
removed from the substrate, essentially a rectangular waveguide is configured. Therefore,
the design of this resulting bandpass waveguide interconnect can be systematically divided
into two steps. The first step is designing the waveguide sidewalls, which are configured by
vias of radius $R$ and center-to-center spacing of $a$, i.e., the lattice constant of the EBG sub-
strate. The unit cell of the substrate can be chosen to be of a square type [8], as indicated
in Fig. 3.2. The limits of the bandgap determines the frequency range at which the signal
propagation is confined within the waveguide section. In the second step, the width of the
waveguide is determined for single mode propagation, \( i.e., \) TE\(_{10}\) mode, while considering the substrate material. This is very close to \( \lambda_g/2 \), which is used for a rectangular waveguide with solid sidewalls. \( \lambda_g \) is the guided wavelength.

![Top View and Side View of an EBG Waveguide-Based Interconnect](image)

**Fig. 3.2** Top view and side view of an EBG waveguide-based interconnect.

To reduce the complexity of the substrate and for ease of fabrication, it is desired to employ as few rows as possible in implementing the waveguide sidewalls. Therefore, by monitoring the leakage of fields through the via sidewalls, an optimum number of rows is determined. The leakage can be measured directly from the total power calculation in (3.1) when neglecting conductor and dielectric losses.

\[
P_{total} = |S_{11}|^2 + |S_{21}|^2
\]  

(3.1)

Fig. 3.3 depicts the total power for two cases where the sidewalls comprise one or two rows of vias. The waveguide dimensions are \( a = 2.54 \) mm, \( R = 0.762 \) mm, \( h = 0.508 \) mm.
mm, $W_g = 7.016$ mm, and $\epsilon_r = 4.4$. The total length of both waveguide sections are 25.4 mm. It is observed that the leakage in both cases is less than 0.4%. However, the two-row case exhibits only 0.1% less leakage compared to the single-row case. This implies that a single row of vias can be efficiently used instead of multiple rows of vias in emulating a solid sidewall. Therefore, the optimum EBG waveguide-based interconnect, as shown in Fig. 3.1, is also referred to as substrate integrated waveguide or laminated waveguide. For the rest of the thesis, the terms, substrate integrated waveguide (SIW) and waveguide interconnect, will be used interchangeably to refer to this type of interconnect.

![Fig. 3.3](image.png) The total power derived from simulated $S_{11}$ and $S_{21}$ of the EBG-based waveguide for lossless single-row and two-row cases.

### 3.3.1 Design Example

In the first case study, a section of the waveguide interconnect is designed to operate in the ku-band (12–18 GHz). An FR4 substrate with dielectric constant ($\epsilon_r$) of 4.4 and substrate thickness (h) of 0.508 mm is used for this purpose. The waveguide sidewalls should be designed to create a bandgap that extends beyond the operating range of 12–18 GHz. By considering the square unit cell presented in Fig. 3.2 and employing an eigenmode solver, the Brillouin diagram for the EBG substrate is generated. The dimensions of the unit cell are chosen as $a = 2.54$ mm and $R = 0.762$ mm to obtain the desired bandgap. From Fig. 3.4, it can be observed that the first bandgap exists from DC to 43.5 GHz. The horizontal axis represents the possible directions of the wave-vector as dictated by the first Brillouin zone. Due to the symmetric nature of this 2-D periodic structure in the x-y plane, its
lattice unit cell is considered the square shown in the inset of Fig. 3.4. A description of the Brillouin zone for a square lattice is included in Appendix A. More details on mapping of the wave-vectors to the irreducible Brillouin zone and generation of the dispersion diagrams can be found in [8]. From simulations with different sizes of EBG unit cells, it is observed that, for a fixed via spacing, the higher bandgap can be achieved by increasing the diameter of the via.

The waveguide section is required to yield a TE\textsubscript{10} cutoff frequency below 12 GHz to allow confined signal propagation over the entire ku-band. Since the waveguide sidewalls are not solid conductors, the cutoff frequency of the TE\textsubscript{10} mode is determined by calculating the effective width of the waveguide, labeled as $W_{eff}$ in Fig. 3.2, instead of its physical width ($W_g$) by using (3.2).

$$W_{eff} = W_g + 2R - \frac{4R^2}{0.95a}$$  

(3.2)

The above expression was derived in [93] based on the least square fitting of a set of fullwave simulation data, and is valid for $a < \lambda_o \cdot \sqrt{\epsilon_r}/2$ and $a < 8R$. From the cutoff frequency constraints, $W_g$ is found to be 7.016 mm. By using (3.2), $W_{eff}$ is found to be 7.58 mm yielding the cutoff frequency of 9.4 GHz for the TE\textsubscript{10} mode. To verify this, the cutoff frequency is found from the propagation constant ($\beta$) simulated by a fullwave solver. $\beta$ can be derived from 3.3, which has been investigated experimentally in [94].

$$\beta = -\frac{\angle S_{21,\text{unwrapped}}}{L}$$  

(3.3)

$\angle S_{21,\text{unwrapped}}$ is the unwrapped phase of the $S_{21}$-parameter, and $L$ is the length of the line. In addition, $\beta$ of a conventional waveguide with solid sidewalls for widths of 7.016 mm and 7.58 mm are calculated using the same approach. From the graph of the three propagation constants shown in Fig. 3.5, it is observed that $W_g$ cannot be used, as it tends to overestimate the cutoff frequency. The $W_{eff}$ derived from (3.2) gives a very good approximation of the cutoff frequency.
Fig. 3.4  The Brillouin diagram of the EBG unit cell shown in Fig. 3.2.

Fig. 3.5  Comparison of the propagation constants of the substrate integrated waveguide of the design example ($W_g = 7.016$ mm) and solid-wall waveguide of widths: 7.016 mm and 7.58 mm.
3.4 Transmission Characteristics

In order to evaluate the transmission characteristics of the waveguide, microstrip lines and striplines are used as the benchmark structures. The first case study utilizes a lossy FR4 substrate with $\epsilon_r = 4.4$ and $\tan\delta = 0.02$. The waveguide has the same dimensions as that of the one in the design example described in Section 3.3.1. For microstrip and stripline, each structure is designed to have a characteristic impedance of 50 $\Omega$. All three structures have the same length of 25.4 mm. The incurred losses in these structures, as depicted in Fig. 3.6(a), are found at 18 GHz for various substrate thicknesses ranging from 0.1 mm to 1.5 mm, which are common for modern electronic substrates. The substrate thickness in the stripline case is defined as the distance between the two ground planes. From Fig. 3.6(a), it is observed that the microstrip exhibits the lowest transmission loss, and the waveguide has the highest for the thicknesses over 1 mm. However, the losses in striplines dominate for the thicknesses less than 1 mm. The losses in microstrip and waveguide are comparable when the thickness decreases to 0.1 mm. In practice, in multilayer substrates, microstrip lines are usually embedded in the dielectric layers. Therefore, the embedded microstrip is also investigated in these simulations. In the results shown in Fig. 3.6, the substrate thickness for the embedded case is defined as the thickness of the dielectric layer below the microstrip, while the total thickness, which includes the microstrip superstrate, is twice this value. In the same figure, it is observed that the loss performance of the embedded microstrip is comparable to that of the waveguide. In fact, the losses in the waveguides are less than those of an embedded microstrip when the thickness decreases below 0.4 mm.

The second case employs a low-loss TMM6 substrate with $\epsilon_r = 6$ and $\tan\delta = 0.0023$. The desired operating frequency range is between 35–40 GHz. The waveguide sidewalls have been re-designed with $a = 0.8$ mm and $R = 0.2857$ mm to induce a bandgap that spans beyond the operating frequency band from DC to 123 GHz (calculated from an FEM solver). For the waveguide cross section, $W_g$ is chosen to be 2.1686 mm for the TE$_{10}$ mode to start propagating above 26.5 GHz. The simulated results at 40 GHz are shown in Fig. 3.6(b). In this case, it is clear that the stripline has the worst loss performance whereas the microstrip has the lowest loss down to the substrate thickness of 0.2 mm. The losses in the embedded microstrip are comparable to those of the waveguide, however, the waveguide shows less losses for the thicknesses smaller than 0.7 mm.

Although a microstrip line, in general, has the lowest insertion loss for thicker substrates,
its mode purity is not as good as what is offered by a waveguide structure. In fact, higher order modes can be present in the form of leaky waves in open and embedded microstrip structures [95]. In contrast, for the same substrate height, the waveguide can be designed to propagate only the first fundamental mode, \( i.e., \ TE_{10} \) mode.

As presented in this section, the waveguide interconnect exhibits lower losses in thin substrates. Therefore, the waveguide is the most suitable candidate for implementation in multilayer packaging where stacks of relatively thin substrates are usually required.

![Comparison of losses in SIW, embedded microstrip line, microstrip line and stripline for different substrate thicknesses. The conductor in the model is copper. (a) Simulated at 18 GHz for an FR4 substrate. (b) Simulated at 40 GHz for a TMM6 substrate.](image)

### 3.5 Bend Geometry

Bend is a widely used signal routing topology. Therefore, various substrate integrated waveguide bends are developed and evaluated in this section. All of the waveguide dimensions and parameters used herein are the same as those determined in the design example of Section 3.3.1. Unless otherwise stated, conductor and dielectric losses are included in all simulations. The conductor is copper, and the dielectric material used for the substrate is FR4 \((\varepsilon_r = 4.4 \ and \ \tan\delta = 0.02)\).

The first studied structure is a right-angle bend whose waveguide width is 7.016 mm. Therefore, its \( TE_{10} \) and \( TE_{20} \) cutoff frequencies are 9.4 GHz and 18.8 GHz, respectively.
3.5 Bend Geometry

Fig. 3.7(a) shows the top view of the magnitude of the electric field inside the bend at 18 GHz. It can be observed that at this frequency only the TE$_{10}$ wave propagates along the uniform section. However, the TE$_{20}$ mode appears to be excited at the bend. Since the corner width is 10.5 mm, the new cutoff frequency of the TE$_{20}$ mode is now 12.9 GHz instead of 18.8 GHz. As a result, an input wave of 18 GHz will be mostly coupled to the TE$_{20}$ mode at the bend discontinuity. When this TE$_{20}$ mode continues after the bend to the output port, it is heavily attenuated due to the higher TE$_{20}$ cutoff frequency of the uniform section. This observation is confirmed by the S-parameter plot in Fig. 3.7(b), as the signal transmission starts to decline after 15 GHz. The ripple in the $S_{11}$-parameter can be attributed to the mismatches and reflections in the waveguide bend structure.

![Fig. 3.7 Simulated right-angle bend. (a) Geometry and plot of the magnitude of the TE$_{10}$ electric field at 18 GHz. (b) Magnitudes of $S_{11}$ and $S_{21}$ for the TE$_{10}$ mode.](image)

The common method of compensation for the discontinuity of a microstrip bend is to miter its corner. The commonly practiced mitering angle is 45 degrees. The same idea is applied to the waveguide-under-study as depicted in the chamfered bend of Fig. 3.8(a). Since the width at the corner is now smaller than that of the uniform section (4.5 mm as opposed to 7.016 mm), the TE$_{10}$ cutoff frequency at the corner is increased to 14.1 GHz. As a result, it is expected to observe much less transmission below 14.1 GHz. This is indicated in the plot of the magnitude of the electric field in Fig. 3.8(a) for 12 GHz. The S-parameter plot of Fig. 3.8(b) also confirms higher insertion loss below 14 GHz.

For a waveguide-type structure, it is important to maintain the width throughout the
bends and angled geometries. Therefore, the three compensated bend structures as shown in Fig. 3.9 are suggested. In the first design, bend A in Fig. 3.9(a), a via is added at the right-angle corner of the left sidewall in order to reduce the width. The second structure, bend B in Fig. 3.9(b), is a chamfered bend in which a via is removed from the right-angle corner of the right sidewall. The third design or bend C has a rounded corner, as shown in Fig. 3.9(c). From the simulations presented in Fig. 3.10, it is observed that all the three bends have comparable insertion losses (within 0.3 dB between 12–18 GHz). In addition, a uniform section of the waveguide with the same total length (92.36 mm) as those of the bends is simulated. From Fig. 3.10, it is observed that the waveguide has a comparable insertion loss with that of the all three bends. These compensated bends have shown to be very effective in transmitting signals to the output port. The choice of the compensation method will ultimately depend on the fabrication constraints.

A waveguide bend is expected to contain signal propagation better than that of a microstrip line. In the next study, power leakage is monitored to evaluate these two types of bend interconnects. Both conductor and dielectric losses are neglected in these cases in order to calculate the leakages directly from (3.1). According to [96], the microstrip bend geometry depicted in the inset of Fig. 3.11 provides the best transmission characteristic when the indicated dimensions are used. From the total power derived from the S-parameter simulations (shown in Fig. 3.11), it is observed that all the compensated waveguide bends

**Fig. 3.8** Simulated chamfered bend. (a) Geometry and plot of the magnitude of the TE$_{10}$ electric field at 12 GHz. (b) Magnitudes of $S_{11}$ and $S_{21}$ for the TE$_{10}$ mode.
3.5 Bend Geometry

Fig. 3.9  Suggested compensated bend structures showing the magnitudes of the propagating TE$_{10}$ electric field at 18 GHz. (a) Bend A: right-angle bend with a via added at the right-angle corner of the left sidewall. (b) Bend B: chamfered bend with a via removed from the right-angle corner of the right sidewall. (c) Bend C: rounded bend.

have leakages less than 1%. However, the leakage from the microstrip bend is between 6% and 11% over the same frequency range. In addition, it is found that a stripline bend has a comparable performance (leakages less than 1%) as those of the waveguide bends. Hence, it can be concluded that the waveguide bends are more efficient in providing signal transmission compared to the microstrip bend.
3.6 Crosstalk between Two Waveguide Interconnects

Crosstalk has become an important consideration in designing high-performance electronic systems especially as the operation frequencies increase. The cross-coupling effect is much more pronounced in compact systems, and could lead to a higher risk of false detections and malfunctioning. Waveguides are shielded structures and, therefore, offer an excellent crosstalk immunity. In this section, crosstalk in multiple interconnect structures, including
3.6 Crosstalk between Two Waveguide Interconnects

SIWs and microstrip lines, is investigated. For a fair comparison, the studied structures should have the same lateral dimension. This feature size is defined as the total width ($W_{total}$) of two adjacent interconnects (microstrips or waveguides) measured from their outer edges, as shown in Fig. 3.12(a) and the inset of Fig. 3.12(b).

Earlier, the waveguide dimensions were designed to operate in the ku-band. Consequently, $W_{total}$ of the two waveguide interconnects is calculated to be 18.604 mm. This number is too large for a benchmark microstrip structure to show any significant couplings. To see the crosstalk between the two microstrips, the operation frequency range is increased to 35–40 GHz, thus, $W_{total}$ is reduced. Each waveguide interconnect has the following parameters: $a = 0.8$ mm, $R = 0.2857$ mm, $h = 0.508$ mm, and $\epsilon_r = 6$. This yields a bandgap frequency extending from DC to 123 GHz. The waveguide section has a cross-sectional width ($W_g$) of 2.1686 mm, resulting in the $TE_{10}$ cutoff frequency of 26.5 GHz, using (3.2). The conductor is copper, and the substrate has tan$\delta$ of 0.0023 at 10 GHz.

Fig. 3.12(a) shows the two waveguide interconnects with 28 mm in length. The magnitude of the electric field where the input signal is applied to port 1 is also presented in Fig. 3.12(a) showing negligible coupling between the waveguides at 40 GHz. This is confirmed by the near-end ($S_{31}$) and far-end ($S_{41}$) couplings of less than 65 dB and 50 dB, respectively (see Figs. 3.12(b) and 3.12(c)). Next, a two-microstrip line structure with the same $W_{total}$, i.e., 6.0514 mm, are simulated. Each microstrip has a width of 0.76 mm resulting in a single-ended characteristic impedance of 50 $\Omega$. It is observed that $S_{31}$ of both structures are very comparable. However, the far-end crosstalk of the multiple waveguide geometry is at least 6 dB better than that of the two-microstrip structure. In the crosstalk scenario inspected in this section, it can be observed that the crosstalk between the waveguides is significantly less than the crosstalk between microstrips with the same $W_{total}$.

A two-stripline structure of the same feature size was also investigated. The width of the line is 0.68 mm for the superstrate and substrate heights of 0.508 mm. For a relatively thin substrate thickness, the electric field on the stripline is confined to the vicinity of the transmission line. As expected, fullwave simulations show that the near-end and far-end crosstalks between the striplines are insignificant and below -84 dB and -89 dB, respectively, mainly due to wide spacing. Therefore, advantages of utilizing the waveguide interconnect instead of stripline is not very evident in this case. However, as the operation frequency increases, cross-coupling between these striplines will increase significantly.
3.7 Waveguide Transitions

As mentioned earlier in Section 3.2, transitions are very important for integrating the waveguide interconnects with active and passive circuitries. A microstrip line is one of the most common planar lines used in printed circuit boards. Therefore, efficient passive transition sections are required for integrating the waveguide interconnects with microstrip circuits. The coplanar microstrip-to-waveguide transition of Fig. 3.13(a) has been shown to be very effective and broadband [65]. For vertical connectivity, the via transition as shown in Fig. 3.13(b) can be utilized. Furthermore, the waveguides can be vertically interconnected by an aperture in their common conductor surface, as depicted in Fig. 3.13(c). These three transition structures are chosen for system integration studies in this thesis. The CPW-to-SIW transition is modeled and fully developed in [67]. The coplanar transition is originally introduced and investigated in [65], it is extensively used in this
thesis. To adapt it to our waveguide structures, parametric simulations are conducted in the subsequent section to offer a guideline for faster design. The remaining transition structures will be investigated in details in Chapter 4.

![Fig. 3.13 Transition geometries.](image)

3.7.1 Coplanar Microstrip-to-Waveguide Transition

The coplanar microstrip-to-waveguide transition is essentially a tapered microstrip line connecting a microstrip of width, $W$, to the waveguide of width, $W_g$, as shown in Fig. 3.14. Since $W$ is usually fixed for a microstrip line of a certain characteristic impedance, the two main design parameters are $W_t$ (transition width) and $L_t$ (transition length). The design of this type of transition is mostly realized by optimizing the feature sizes while monitoring the fullwave simulation results [65]. Nonetheless, it is possible to estimate the initial values of these parameters in order to narrow down the range of parametric simulations. It is concluded from several test cases that the initial values of $W_t$ and $L_t$ in the optimization process can be estimated from $W_t/W_g \simeq 0.4$ (found as a reasonable starting point from
simulations of a number of structures), and \( \lambda/2 < L_t < \lambda \). \( \lambda \) is the wavelength of the propagating quasi-TEM mode in the microstrip line. In order to speed up the optimization process, these observations have been employed in the transition design.

The first case study uses the waveguide described in Section 3.3.1. For all of the optimization results, dielectric and conductor losses are not included in order to observe the effect of transition discontinuity. Using the initial guess of \( W_t/W_g = 0.4 \), \( W_t \) is chosen to be 2.8 mm. Since \( \lambda \) of the wave in the microstrip at 15 GHz is approximately 10 mm, \( L_t \) is varied from 5 mm to 9 mm. Fig. 3.15(a) shows a set of magnitude plots of \( S_{11} \) for the geometry shown in Fig. 3.14 when different values of \( L_t \) are considered. It is observed that the optimum matching, \( i.e., \) return loss, is obtained over the entire frequency range when \( L_t = 8 \) mm. Next, \( W_t \) is refined by starting the initial guess of 2.8 mm and using the found optimum \( L_t \). The magnitudes of \( S_{11} \) for different values of \( W_t \) are also shown in Fig. 3.15(b). The transition has the best reflection characteristic when \( W_t = 3 \) mm.

The second case study is for the waveguide interconnect operating between 35–40 GHz.
In this scenario, the substrate has the dielectric constant of 6, and the waveguide has the following dimensions: \( a = 0.8 \, \text{mm} \), \( h = 0.508 \, \text{mm} \), \( W = 0.76 \, \text{mm} \), \( W_g = 2.1686 \, \text{mm} \), and \( D = 0.5714 \, \text{mm} \). The cutoff frequency for the TE\(_{10}\) mode is 26.5 GHz. Again from \( W_g \), \( W_t \) is estimated to be around 0.87 mm. Since \( \lambda \) of the wave in the microstrip is approximately 5 mm at 37.5 GHz, \( L_t \) is varied between 2.6–4 mm. From the parametric simulations shown in Fig. 3.16, it can be observed that the optimum dimensions for \( W_t \) and \( L_t \) are 0.84 mm and 2.8 mm, respectively.

![Fig. 3.15](image_url)  
**Fig. 3.15** Magnitudes of \( S_{11} \) obtained from parametric fullwave simulations of the coplanar transition \((\epsilon_r = 4.4)\). (a) Different values of \( L_t \) \((W_t = 2.8 \, \text{mm})\). (b) Different values of \( W_t \) \((L_t = 8 \, \text{mm})\).
3.8 Shielding the Microstrip Section of Coplanar Transition

In this section, coplanar microstrip-to-waveguide transitions configured in a multiple interconnect structure are improved in order to reduce their crosstalk level. This is achieved by inserting via fence geometries between the transitions, which will be discussed in the following subsections.

3.8.1 Continuous Via Fence

The common method to reduce coupling between the adjacent striplines and microstrip lines is by inserting via fences. Unlike striplines, microstrip lines cannot be completely shielded by the via fences, as the electromagnetic fields also spread in the region above the fence. Therefore, a modified via fence was proposed as an effective shielding structure between microstrip lines [97]. This modified via fence, which is called continuous via fence, incorporates a metal trace that connects the top ends of all vias. Fig. 3.17(a) shows two microstrip lines separated by a continuous via fence. Fullwave simulations are performed for the following three multiple microstrip structures: microstrip lines without via fence, microstrip lines with regular via fence, and microstrip lines with continuous via fence (shown in the inset of Fig. 3.17(b)). The dimensions and the substrate parameters of the microstrip lines and vias are as follows: \( R_v = 0.2857 \) mm, \( S = 2 \) mm, \( W = 0.76 \) mm.
mm, $\epsilon_r = 6$, and $\tan\delta = 0.0023$. The width of the strip ($W_s$) that connects vias in the via fence is chosen to be 20% wider than the diameter of the vias. From $S_{31}$ plots of Fig. 3.17(b), it can be concluded that the near-end crosstalk of all of the three test structures are quite comparable; while, a slightly better performance is obtained when a continuous via fence is placed. In Fig. 3.17(c), it is clearly obvious that the forward coupling in the case with a continuous via fence is improved by more than 6 dB compared to the structure without a via fence. It is also important to note that $S_{41}$ of the two microstrips without a via fence is slightly better than the structure with a regular via fence. This indicates that the regular via fence inspected here adds more coupling between the microstrip lines rather than reducing it.

### 3.8.2 Crosstalk in Multiple Waveguide Interconnects with Coplanar Transitions

The far-end coupling ($S_{41}$) between multiple waveguides is shown to be very small or negligible. However, when the coplanar microstrip-to-waveguide transitions are added, the coupling between the transition sections are very likely to degrade the crosstalk immunity between the interconnects. This effect can worsen at high frequencies, as the feature size is further reduced. To investigate this, the multiple waveguide geometry with continuous via fences between the transitions is considered, as shown in Fig. 3.18(a).

An increased coupling is observed when the continuous via fence is placed too close to the transition sections. Since the spacing between the transition sections is usually fixed, only the characteristic dimensions of the via fence can be changed in order to minimize the coupling. The width of the strip in the via fence should be chosen as close as possible to the diameter of the via (20% wider than the diameter of the via as recommended in the previous section). It was observed from the fullwave parametric simulations that a slightly larger coupling occurs when the strip is close to the transition sections. Furthermore, as explained earlier, a smaller lattice constant ($a$) also reduces the field leakage through the via wall. Fullwave simulations were conducted to obtain the $S_{31}$ and $S_{41}$ parameters of three different multiple waveguide configurations—without via fences, with regular via fences, and with continuous via fences, as depicted in Figs. 3.18(b) and 3.18(c). The total length of each structure is 30 mm with the following dimensions: $L_m = 5$ mm (length of the microstrip section), $L_w = 20$ mm (length of the waveguide section), and $S = 1.98$
Fig. 3.17  (a) Multiple microstrip lines with $S = 2$ mm. (b) Magnitude of $S_{31}$. (c) Magnitude of $S_{41}$. 
mm (spacing between microstrips). These results are also compared with that of a two-microstrip structure with a continuous via fence having the total length of $2L_m + L_W$ and spacing $S$. The plot of simulated $S_{31}$ parameters shown in Fig. 3.18(b) proves that the near-end coupling of the two waveguide interconnects with continuous via fences is lower than the other studied cases. It is, however, comparable to that of the multiple microstrips with continuous via fences. From Fig. 3.18(c), it can be seen that the magnitude of $S_{41}$ for the case of the two SIW interconnects with regular via fences is at least 2.5 dB worse than that of the structure without any via fences. However, an additional improvement of 4.5–8 dB is observed when a continuous via fence is used. Therefore, the two waveguide interconnects have a better far-end crosstalk performance, i.e., 5.5–8.5 dB in this case, than that of the two adjacent microstrips when the pertinent spacing is comparable.

![Diagram](image)

**Fig. 3.18** (a) Multiple waveguide interconnects with continuous via fences in the transition sections. (b) Magnitude of $S_{31}$. (c) Magnitude of $S_{41}$.
3.8.3 Measurements of Multiple Waveguide Structures

To investigate the effectiveness of the via fence, a multiple waveguide interconnect structure was prototyped in an FR4 substrate, as depicted in Fig. 3.19(a). The waveguide dimensions are the same as those used in the example of Section 3.3.1. Coplanar microstrip-to-waveguide transitions ($W_t = 3$ mm and $L_t = 8$ mm) are employed for connectivity with SubMiniature version A (SMA) connectors. The total length of the structure is 100 mm. The spacing between the coplanar transitions is 7.57 mm, which is dictated by the width of the waveguide. To measure far-end crosstalk, two SMA connectors are attached to both waveguides but on the opposite ends. The remaining ports are terminated by 52-Ω surface-mount resistors. The far-end coupling ($S_{41}$) is measured by an Anritsu 37397D vector network analyzer (VNA) with Short-Open-Load-Thru (SOLT) calibration standards, as shown in Fig. 3.20. It can be observed that -40 dB or less coupling is obtained below the cutoff frequency of the waveguide. In the passband region of the waveguide, however, the far-end coupling is as high as -20 dB. The waveguide is shown to be quite susceptible to crosstalk when coplanar microstrip transitions are included.

In order to reduce coupling between the transitions, via fence structures as discussed in Section 3.8.1 are incorporated between the transitions, as shown in the front and top views in Fig 3.19(b). A 100-mm long multiple waveguide structure containing the via fence geometries as presented in Fig. 3.19(b) was also fabricated in an FR4 substrate having the same dimensions as the previous two-waveguide prototype. The vias in the interleaving fences each has a diameter of 1.524 mm. They are uniformly spaced by $p = 2.54$ mm and are all connected at the top end with a 2-mm wide microstrip ($W_s$). The far-end crosstalk of this prototype is characterized in the same manner as the other two-waveguide structure, and the measured $S_{41}$ coupling is included in Fig. 3.20. It can be observed that significant improvement in the isolation between the two SIWs is obtained when using these via fences. Near-end measurements are not included in this work, as the spacing between the microstrips is too small to accommodate two SMA connectors. Nonetheless, simulation results as shown in Fig. 3.21 show that near-end crosstalk is improved by at least 10 dB within the ku-band when the via fence structures are used to shield the adjacent microstrip transitions.
3.9 Summary

A systematic approach to the design of the substrate integrated waveguide interconnect is presented by employing the electromagnetic bandgap concept. The waveguide structure is designed and optimized for operation in the ku-band while having negligible leakage from the sidewalls. The transmission loss of the waveguide interconnect is also compared with those of common planar lines, i.e., microstrip line, embedded microstrip line, and stripline in both lossy (FR4 at 18 GHz) and low-loss (TMM6 at 40 GHz) substrates. It is found that the waveguide and stripline exhibit the highest losses in thick substrates. However, for thinner substrates, the losses in the waveguide are comparable to that of a microstrip, and even become smaller when the substrate thickness is reduced further.

In addition, this type of waveguide interconnect can be efficiently implemented in a bend geometry while demonstrating a superior performance compared to a microstrip bend. It is found that it is very important to maintain a uniform width along the bend to obtain efficient signal transmission. Therefore, three bend designs are suggested that include
Fig. 3.20 Measured far-end coupling of the fabricated multiple waveguide interconnect prototypes.

Fig. 3.21 Simulated near-end coupling of the fabricated multiple waveguide interconnect prototypes.
3.9 Summary

Chamfered and rounded bend geometries. All of these structures offer similar performances, thus, the ultimate choice of the design depends on the ease of fabrication and layout plan.

For crosstalk analysis, multiple waveguide interconnects are investigated, and very small far-end and near-end couplings are observed. However, when the microstrip-to-waveguide transition sections are added to integrate with planar circuits, the near-end and far-end couplings increase dramatically. Therefore, via fence structures are proposed to be included in the transition sections. The continuous via fence demonstrates the most effective shielding in the coplanar microstrip-to-waveguide transitions. Finally, a general comparison between SIW interconnects, microstrips and striplines is presented in Table 3.1. In this comparison, it is assumed that the stripline is embedded in a homogeneous dielectric. The frequency of operation is considered to be in the microwave range, thus, in the row comparing the physical widths, the width of the SIW renders to be relatively larger. The isolation of the stripline is labeled medium due to lateral openness of the geometry.

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>SIW</th>
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<th>Stripline</th>
</tr>
</thead>
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<td>Medium</td>
<td>Medium</td>
</tr>
<tr>
<td>Loss</td>
<td>Low</td>
<td>High</td>
<td>High</td>
</tr>
<tr>
<td>Dispersion</td>
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<tr>
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<td>Low</td>
<td>Medium</td>
</tr>
<tr>
<td>Physical Width</td>
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<td>Small</td>
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</tr>
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</table>
Chapter 4

3-D Integration of Substrate Integrated Waveguides

4.1 Introduction

Efficient transition sections are important in 2-D and 3-D integration of the waveguide-based interconnects with printed lines and circuits. For connecting the waveguide to circuits on the same layer, a coplanar microstrip-to-waveguide transition [65] can be employed, as presented earlier in Section 3.7.1. However, with the growing trend in multilayer packaging for system miniaturization, 3-D integration schemes are needed. In this chapter, 3-D transitions are introduced for this purpose. The via and aperture transitions are presented in Sections 4.2 and 4.3, respectively. The design guidelines for each transition based on a parametric fullwave simulations are described. Modeling of these transition structures are also presented and validated by fullwave simulations and S-parameter measurements. Furthermore, the accuracy and validity range of these models are investigated. Fullwave FEM simulations are also used as the benchmark for error analysis. This error analysis is also important in examining the validity range of the extracted model with fabrication process variations. Finally, the transition models are evaluated by experimental characterization of the fabricated prototypes.
4.2 Via Transition

4.2.1 Design

Via transition is a common geometry for 3-D signal routing. It can be utilized for vertical connection of a microstrip line to a waveguide in another layer, as shown in Fig. 4.1. The transition has four parameters that need to be optimized: \(d_{pad}\) (via pad), \(d_{wall}\) (distance between the center of the via and the waveguide wall), \(d_{vg}\) (via-ground clearance), and \(R_h\) (radius of the via hole). The optimization process is aimed at maximizing the return loss (minimizing \(|S_{11}|\)) of the transition over a studied operating bandwidth. The waveguide described in Section 3.3.1 will be used in this study.

\[
d_{wall}\text{ is very much dependent on the wavelength of the propagating wave in the waveguide } (\lambda_g), \text{ which should be approximately } \lambda_g/4 \text{ to provide the constructive interference condition for the reflected wave. In this case, } \lambda_g \text{ is 12.4 mm at 15 GHz. Fig. 4.2(a) shows the simulated magnitudes of } S_{11} \text{ for } d_{wall} \text{ from 2.4 mm to 3.2 mm. It is observed that the optimum matching occurs when } d_{wall} \text{ is 2.8 mm, which is very close to the quarter-}
\]

![Fig. 4.1 Via transition geometry.](image-url)
wavelength.

The radius of the via is limited by the width of the microstrip line. The set of magnitude of $S_{11}$ plots depicted in Fig. 4.2(b) reveals that the optimum value for $R_h$ is 0.28 mm. Subsequently, $d_{pad}$ is varied, as depicted in Fig. 4.2(c). Overall, it is observed that $d_{pad}$ of 0.25 mm offers the lowest reflection. This confirms that $d_{pad}$ should not be too large, as there may appear to be more mismatch between the microstrip line and the pad. Finally, for the via-ground clearance, its optimum value is obtained when $d_{vg}$ is 0.32 mm, as shown in Fig. 4.2(d).

### 4.2.2 Modeling

Fullwave simulations are more accurate but more time-consuming, especially when they are conducted for the entire system. Therefore, equivalent circuits are always needed. In the general modeling approach undertaken in this section, the transition structure is divided into several smaller sections that can be represented by using transmission line and lumped element circuits. Since a transition is usually connected to uniform sections of microstrip and waveguide interconnect, their equivalent S-parameters are cascaded with the model of the transition section in circuit simulation. The via transition can be modeled as a combination of three well-known circuit models, each representing a section of transition shown in Fig. 4.3(a).

The first section from points A1 to B1, as marked in Fig. 4.1, is a microstrip via discontinuity. The LC Π-equivalent circuit presented in [98] is employed as the base architecture to extract the model for this section. Since only the top portion of the via is considered, only a half Π-circuit shown by $L_v$ and $C_v$ in Fig. 4.3(a) is used in the model. Several attempts have been made to model via holes in literature. Some of these approaches are based on fullwave methods, such as Finite-Difference Time-Domain [99,100], Spectral-Domain Analysis [101], and Mode-Matching [102]. A quasi-static approach has been studied in [98], which shows less accuracy at high frequencies. In spite of all of these numerical models, there are no closed-form formulas available that can approximate the values for $L_v$ and $C_v$ in this particular LC model. $L_v$ in some cases can be roughly calculated from inductance formulas in [103,104]. $C_v$ is, however, mainly derived from field simulations. A fullwave study showed that the rough approximation of $L_v$ from formulas even in combination with field simulations for $C_v$ will result in low prediction accuracy because the mode conversions
Fig. 4.2  Parametric fullwave simulations of the via transition design parameters shown in Fig. 4.1. Default parameter values: $d_{pad} = 0.25$ mm, $d_{wall} = 2.8$ mm, $d_{vg} = 0.3$ mm, and $R_h = 0.28$ mm. (a) Magnitudes of $S_{11}$ for different values of $d_{wall}$ (b) Magnitudes of $S_{11}$ for different values of $R_h$. (c) Magnitudes of $S_{11}$ for different values of $d_{pad}$. (d) Magnitudes of $S_{11}$ for different values of $d_{vg}$. 
that happen at the microstrip via discontinuity is not fully accounted for. Only a fullwave approach considers mode conversions at discontinuities. Therefore, in this work, $L_v$ and $C_v$ are extracted at a single frequency point from fullwave simulations. It is important to note that these parameters are not extracted from the fullwave simulation of the entire structure shown in Fig. 4.1, which is quite complex due to the existence of via walls. $L_v$ and $C_v$ are extracted from a simpler structure similar to the one in [98], which is essentially a via-hole through ground plane connecting microstrip lines on different layers. This method of determining $L_v$ and $C_v$ has no significant simulation cost and results in excellent accuracy, as indicated in the error analysis of Section 4.2.3.

The second section that starts from point B1 is the lower half of the via, which is represented by the available model for a metal post in a waveguide. The circuit parameters of this section are determined from available formulas in [105]. Finally, the shorter section of the waveguide with the closed end, as shown from points B1 to C1, is modeled by a short-circuited transmission line stub with $d_{wall,eff}$ length. $d_{wall,eff}$ is the distance between the via and the effective location of the waveguide’s end-wall. The input impedance of this section can then be calculated from (4.1).

$$Z_{in,wall} = jZ_{wg} \tan \beta_{wg} d_{wall,eff}$$  \hspace{1cm} (4.1)

$\beta_{wg}$ is the phase constant of the waveguide, and $Z_{wg}$ is the TE$_{10}$ mode waveguide impedance defined by the power-current relation [67], which is found from fullwave simulations. The power-current relation for calculating the waveguide impedance is given in (4.2).

$$Z_{wg} = \frac{P}{I^2}$$  \hspace{1cm} (4.2)

$P$ and $I$ are power and current, respectively. In this manner, the short waveguide section is modeled by the input impedance of a shorted transmission line with a frequency dependent characteristic impedance. $Z_{in,wall}$ is represented in the circuit simulator by a reactive component that can be inductive or capacitive with changing frequency.

For model validation, the test structure shown in Fig. 4.1 is considered with FR4
material \((\epsilon_r = 4.4 \text{ and } \tan\delta = 0.02)\) as the microstrip substrate and the dielectric material filling the waveguide. The waveguide is designed to operate in the ku-band; therefore, as explained in Section 4.2.1, the via diameter, spacing and waveguide width are designed accordingly, and \(a = 2.54 \text{ mm}, D = 1.524 \text{ mm}, \text{ and } W_g = 7.016 \text{ mm}\) are calculated. The uniform microstrip line connected to the transition has a characteristic impedance of 50 \(\Omega\) \((W = 0.97 \text{ mm} \text{ and } h_1 = h_2 = 0.508 \text{ mm})\). The length of the microstrip line, measured from the input end to the center of the via, is 7.8 mm. The total length of the structure measured from the input to the output port is 22.018 mm. The dimensions of the via transition are \(d_{pad} = 0.25 \text{ mm}, d_{wall} = 2.8 \text{ mm}, R_h = 0.28 \text{ mm}, \text{ and } d_{vg} = 0.32 \text{ mm}\) according to earlier parametric simulations. The values for the components in the equivalent model are calculated in the 12–18 GHz frequency range; \(L_v\) changes from 0.207 nH to 0.147 nH, \(C_v\) and \(L_p\) increase from 0.208 pF to 0.257 pF and 0.0616 nH to 0.0713 nH, respectively, while \(C_p\) decrease from 27.04 pF to 12.19 pF. This circuit connects the uniform microstrip line to the rectangular waveguide with \(W_{eff}\) width. In the circuit simulation test-bench, the microstrip and waveguide are terminated to 50 \(\Omega\) and \(Z_{wg}\), respectively. The S-parameters from circuit simulation are compared with the fullwave simulation of the structure shown in Fig. 4.1. As depicted in Fig. 4.3(b), both set of S-parameter results have a very good correlation.

### 4.2.3 Error Analysis

To examine the accuracy and validity range of the extracted via transition model, \(d_{pad}, d_{wall}, R_h, \text{ and } d_{vg}\) are separately varied between \(\pm 20\%\) of their original values. This range is large enough to cover most fabrication tolerances. For instance, a typical value of the etch tolerance is 0.0203 mm, which represents only 2.1\% of the line width. The error in prediction of the S-parameter values by using the circuit model is computed by (normalized) comparison with fullwave simulations, as shown in (4.3) formula. In a well matched situation, \(|S_{11,\text{fullwave}}|\) can have a very small number–close to zero. Particularly, very large ratios will result even with a very slight shift in frequency. Therefore, the error benchmark using \(S_{11}\) is not considered in this study, and only \(S_{21}\) is used in the error analysis.

\[
\%\text{Error} = \frac{|S_{21,\text{model}}| - |S_{21,\text{fullwave}}|}{|S_{21,\text{fullwave}}|}
\]  

(4.3)
Fig. 4.3 Modeling of the via transition. (a) The equivalent circuit. (b) Model validation with fullwave S-parameter simulations.
4.2 Via Transition

In this model accuracy test, the frequency range of operation is extended from 10 GHz to 28 GHz while all the original geometrical parameters optimized in Section 4.2.1 are considered. This frequency band corresponds roughly to the validity range of post in waveguide model, $2W_{eff}/3 < \lambda < 2W_{eff}$, as stated in [105]. The extracted circuit values representing the via transition model, i.e., $L_p$, $C_p$, $L_v$ and $C_v$, are shown in Fig. 4.4. Some comparison of fullwave and circuit $S_{11}$- and $S_{21}$-parameters are depicted in Fig. 4.5. The predicted $S_{21}$ errors are computed and presented in Fig. 4.6. These results are only plotted up to 22 GHz, as the predicted errors become too large beyond this frequency. For the frequency range of 12–18 GHz, the parametric studies demonstrated that the developed model remain reasonably accurate, with maximum 5.3% error in prediction of $S_{21}$ when each geometrical parameter changes within ±20% of its original value. For example, when $R_h$ is varied between 0.224–0.336 mm, the error in predicting $S_{21}$ is within 4.6%. The sensitivity of $S_{21}$ to the placement of the via post in the waveguide is almost similar to the previous case, as the maximum error of 5% is obtained when $d_{wall}$ changes from 2.24 mm to 3.36 mm. Variations of the radius of via pad and via-ground clearance, i.e., $d_{pad}$ and $d_{vg}$, also showed a similar error, on the order of 5.3%, with ±20% change of each of these dimensions. Over this frequency range, it can be observed that the via transition model performance is very sensitive to $d_{vg}$. However, in a wider frequency band, it is more sensitive to $d_{wall}$. Finally, comparison of fullwave and circuit simulations shows that the extracted model is valid across 10.35–19.10 GHz frequency range with less than 15% error.

4.2.4 Experimental Validation

To investigate the via transition experimentally, the test structure with total length of 100 mm was prototyped using an FR4 substrate. The via-transition prototype, as shown in Fig. 4.7(a), has two of the transition sections shown in Fig. 4.1 to provide connection to the input/output SMA ports. Standard SMA connectors were attached to the structure to measure the scattering parameters. The S-parameters were measured by an Anritsu 37397D vector network analyzer. The SMA connectors are de-embedded in comparison of measurement and simulation results. The model used for circuit simulations contain two via-transition representative circuits with the same component values indicated in Section 4.2.2. Fig. 4.7(b) depicts the magnitudes of measured and simulated S-parameters. Excellent agreement between circuit simulation and fullwave results is observed. These
Fig. 4.4  Equivalent circuit values of the via transition model. (a) $L_p$.  (b) $C_p$.  (c) $L_v$. (d) $C_v$.  

---

*3-D Integration of Substrate Integrated Waveguides*
Fig. 4.5  Via transition model validation with fullwave simulations. (a) $d_{pad} = 0.3$ mm. (b) $d_{wall} = 3.36$ mm. (c) $R_h = 0.336$ mm. (d) $d_{vg} = 0.384$ mm.
Fig. 4.6  Error analysis of the via transition model. (a) Variations in $d_{pad}$. (b) Variations in $d_{wall}$. (c) Variations in $R_h$. (d) Variations in $d_{vg}$. 
results closely follow the measurements demonstrating the accuracy and applicability of the developed model.

Fig. 4.7  Experimental validation of the via transition model. (a) Fabricated prototype. (b) Magnitudes of $S_{11}$ and $S_{21}$.

4.3 Aperture Transition

4.3.1 Design

In many routing scenarios, it may be required to interconnect waveguides of different layers. An aperture coupling can be employed as a method for waveguide-to-waveguide transition in these situations. For 3-D integration of two SIWs, the aperture transition shown in Fig. 4.8 is employed, which shows an aperture coupling between two waveguides placed in a parallel orientation. The design parameters are $l_a$ (aperture length), $d_{bw}$ (distance between the aperture to the bottom wall), $d_{tw}$ (distance between the aperture to the top wall), and $W_a$ (aperture width).
Since $\text{TE}_{10}$ is the desired mode of excitation in this case, the aperture length should cover most of the width of the waveguide in order to couple most of the energy into the adjacent layer. The simulation results of Fig. 4.9(a) confirms this comment, as the best matching occurs at $l_a = 6.5$ mm (note: $W_g = 7.016$ mm). In the case of aperture width, it is observed that the width should be as small as possible (see Fig. 4.9(b)). However, $W_a$ is limited by the manufacturing tolerances. Here, $W_a$ is optimized to 0.25 mm to achieve a maximum return loss. Finally, from series of fullwave simulations, it is observed that the aperture should be placed as close as possible to the waveguide wall. From Figs. 4.9(c) and 4.9(d), it can be concluded that $d_{tw}$ and $d_{bw}$ should be both 0.2 mm for the best performance.

### 4.3.2 Modeling

The suggested model for the aperture transition is composed of the equivalent circuit for the aperture and two short waveguides with one closed end, as shown in Fig. 4.10(a). The rectangular aperture indicated by B2 in Fig. 4.8 is represented by the available model for the aperture coupling in rectangular waveguides. The circuit parameters of this model are obtained from the closed-form expressions found in [105]. It is assumed here that the
Fig. 4.9 Parametric fullwave simulations of the aperture transition design parameters shown in Fig. 4.8. Default parameter values: $l_a = 6$ mm, $W_a = 0.5$ mm, and $d_{tw} = d_{bw} = 0.2$ mm. (a) Magnitudes of $S_{11}$ for different values of $l_a$ (b) Magnitudes of $S_{11}$ for different values of $W_a$. (c) Magnitudes of $S_{11}$ for different values of $d_{tw}$. (d) Magnitudes of $S_{11}$ for different values of $d_{bw}$.
aperture length, $l_a$, is equal to the waveguide width. The short waveguide sections, labeled by A2–B2 and B2–C2, and terminated to the transverse end walls, are modeled by short-circuited transmission lines as discussed in Section 4.2.2. The overall circuit model is shown in Fig. 4.10(a).

To validate the model, the structure shown in Fig. 4.8 is simulated by fullwave solver as the benchmark. The waveguides have the same dimensions as the waveguide described in Section 4.2.2. The total length, measured from the input of the upper waveguide to the output of the lower waveguide is 55.88 mm. The aperture transition has the following dimensions: $W_a = 0.25$ mm, $l_a = 7$ mm, and $d_{tw,eff} = d_{bw,eff} = 0.477$ mm. Using the formulas given in [105], the value of the circuit components and their variation range with frequency (from 12 GHz to 18 GHz) are calculated; $L_a$ drops from 41.64 nH to 9.75 nH, $L_b$ decreases from 3.03 nH to 0.704 nH, and $C_a$ increases from 4.22 fF to 8.02 fF. The transition model is cascaded with the S-parameter representation of the rectangular waveguide at the input and output sides in circuit simulations. The resulting overall S-parameters are compared with the fullwave simulation of the entire structure, as presented in Fig. 4.10(b). It can be observed that an excellent correspondence between the fullwave results and the model simulations is achieved.

4.3.3 Error Analysis

To determine the accuracy and validity range of the extracted aperture transition model, $W_a$ and $d_{tw}$ are varied one at a time within ±20% of their original values. It is assumed that $d_{tw}$ and $d_{bw}$ are changed by the same amount at the same time. According to [105], the model for aperture transition is applicable when $2h/\lambda_g < 1$, which yields the validity range of up to 141 GHz for the present structure. In this study, the frequency range of simulations is limited to be 10–30 GHz, which is similar to that of the via transition case. The extracted circuit values of the model, i.e., $L_a$, $L_b$, and $C_a$, are shown in Fig. 4.11. Some comparison of fullwave and circuit $S_{11}$- and $S_{21}$-parameters are depicted in Fig. 4.12. The error predictions in $S_{21}$ are computed and presented in Fig. 4.13. Changing $W_a$ or $d_{tw,eff}$ at a time within ±20% of its original value, while the other parameter is fixed, results in 3% or 2% error, respectively, in $S_{21}$ prediction over 12–18GHz frequency range. It can be observed that the aperture transition model performs reasonably well over the studied range of $d_{tw,eff}$. However, it is slightly more sensitive to $W_a$ variations, which is depicted in
4.3 Aperture Transition

Fig. 4.10 Modeling of the aperture transition. (a) The equivalent circuit. (b) Model validation with fullwave S-parameter simulations.
Fig. 4.13. Finally, comparison of fullwave and circuit simulations shows that the extracted model is valid between 10.1–28 GHz and beyond with less than 15% error.

![Graphs showing L_a, L_b, and C_a values for different W_a values across frequency (GHz).](image)

Fig. 4.11 Equivalent circuit values of the aperture transition model. (a) $L_a$. (b) $L_b$. (c) $C_a$.

### 4.3.4 Experimental Validation

The second prototype was fabricated to evaluate the aperture-transition model. The 100-mm long structure was also prototyped in an FR4 substrate. To attach SMA connectors to this test board, two microstrip coplanar transitions are employed, as shown in Fig. 4.14(a). The microstrip transition sections are connected to the top and bottom plates of the waveguides indicating the input and output ports. To obtain S-parameters from circuit
4.3 Aperture Transition

Fig. 4.12 Aperture transition model validation with fullwave simulations. (a) $W_a = 0.3$ mm. (b) $d_{tw} = d_{bw} = 0.24$ mm.

Fig. 4.13 Error analysis of the aperture transition model. (a) Variations in $W_a$. (b) Variations in $d_{tw}$ or $d_{bw}$. 
simulations, the prototyped structure is modeled by using the equivalent circuit described in Section 4.3.2. The magnitudes of measured and simulated S-parameters are presented in Fig. 4.14(b). This figure also includes S-parameters generated by fullwave simulation of the test structure. Comparison of the three sets of S-parameters attests to the accuracy of the developed model. The main source of difference between the measured and simulated results is attributed to the fabrication errors and the non-ideal contact between the SMA connectors and the test-boards.
Fig. 4.14  Experimental validation of the aperture transition model. (a) Fabricated prototype. (b) Magnitudes of $S_{11}$ and $S_{21}$. 
4.4 Summary

The via and aperture transition structures are investigated for 3-D integration of the waveguide-based interconnects. The via transition is best suited for the vertical integration of a microstrip-to-waveguide transition, and the aperture-type transition is suitable for a 3-D waveguide-waveguide integration. The design of each transition involves determining the geometrical parameters and performing parametric fullwave simulations to achieve the best possible matching condition. The equivalent circuit of each of these geometries is developed and ported to commercial circuit solvers to conduct S-parameter simulations. Modeling is a crucial task in system engineering, as it enables global circuit simulations and design optimization, which eventually reduce the fabrication turn-around time. The validity range and accuracy of the models are evaluated by parametric studies and full-wave simulations. The considered error metric is a measure of the normalized difference between the fullwave and model generated $S_{21}$-parameters. For more than 85% accuracy, the via transition model is shown to be valid between 10.35–19.10 GHz whereas it covers the 10.1–28 GHz range for the aperture transition model. Test structures for the via and aperture transitions were fabricated and characterized by S-parameter measurements. The developed equivalent circuits are employed to model two test-boards and the predicted S-parameters showed good correlation with fullwave simulations and measurements.

Finally, it is concluded that the coplanar transition has the broadest bandwidth with the highest return loss (return loss > 20 dB for the entire frequency band). The via transition is the second best transition with the return loss of less than 20 dB within about 60% of the band. The return loss for the aperture is found to be higher (12–15 dB). Comparison of the performance characteristics of these transitions is summarized in Table 4.1.

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Coplanar Transition</th>
<th>Via Transition</th>
<th>Aperture Transition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Return Loss</td>
<td>High</td>
<td>Medium</td>
<td>Low</td>
</tr>
<tr>
<td>Insertion Loss</td>
<td>Low</td>
<td>High</td>
<td>Medium</td>
</tr>
<tr>
<td>Bandwidth</td>
<td>High</td>
<td>Low</td>
<td>Medium</td>
</tr>
</tbody>
</table>
Chapter 5

High-Speed Data Transmission in Waveguide-based Interconnects

5.1 Introduction

Due to the bandpass characteristic of the waveguide interconnects, driver and receiver must be modified in order to accommodate digital baseband transmissions. In this chapter, design and implementation of these blocks is proposed and discussed in details. In addition, wideband transmission performance of the waveguide interconnect is evaluated through signal integrity analysis. Investigation of mode coupling and dispersion in the waveguide interconnect is studied in Section 5.2. A high-speed data transmission system employing a waveguide-based interconnect as one of its constituents is introduced in Section 5.3. A design guideline, which takes into account of the capability of the system components, is given to aid the system implementation. Characterization of the prototyped waveguide through S-parameter measurements is also included in this section. The first implementation of the waveguide interconnect system for high-speed data transmissions is presented and evaluated experimentally for data rates of 3.125 Gb/s and 5 Gb/s in Section 5.4.

5.2 Signal Integrity Analysis of the Waveguide Interconnect

When substrate integrated waveguide is utilized as an interconnect for broadband and high-speed signaling, two factors seem to constrain its usable bandwidth: dispersion and excitation of higher-order modes. The TE_{10} cutoff and the strong dispersive characteristics
limit the lower end of the bandwidth and mode excitation and power coupling to TE\(_{20}\) and TE\(_{30}\) modes influence the higher frequency region. Therefore, a bandpass characteristic is considered for a waveguide interconnect in which single mode operation exists in the frequency range between TE\(_{10}\) and TE\(_{20}\) cutoff frequencies.

In a typical substrate integrated waveguide, TE\(_{m0}\) modes, \((m = 1, 2, 3, ...\)), are the dominant modes because the substrate thickness is much smaller than the waveguide width \([106]\). Ideally, due to orthogonality, there should be no mode coupling if the sidewalls were solid conductors and there were no discontinuity (see Appendix B for a proof). To investigate this, fullwave simulations are conducted using Ansoft HFSS. Mode coupling coefficients in a substrate integrated waveguide are generated and compared with those of a similar rectangular waveguide with solid walls. The structure shown in Fig. 3.1 is simulated where the waveguide width \(W_g\), i.e., the spacing between the rows of via fences, is considered to be 4.13 mm and \(\epsilon_r = 6.15\). The height of the waveguide is 0.635 mm, and the spacing between the vias \((a)\) is 1 mm. The via diameter is 0.5714 mm. The equivalent solid waveguide simulated for comparison has a width of 4.35 mm.

In the simulation setup, one of the waveguide ports is excited by the fundamental TE\(_{10}\) mode. The electric field vector of the higher order modes, i.e., TE\(_{20}\) and TE\(_{30}\), is monitored at the opposite port. For example, \(S(\text{TE}_{20}:\text{TE}_{10})\) is used to describe the mode coupling when the TE\(_{20}\) wave is detected at the output when the TE\(_{10}\) mode is applied to the input port. As shown in Fig. 5.1(a), for the solid waveguide, it can be seen that the mode coupling between TE\(_{10}\), TE\(_{20}\) and TE\(_{30}\) modes is less than -80 dB in the single mode operation region (14–28 GHz). The isolation is degraded as the frequency increases, i.e., 103 dB at 14 GHz to 55 dB at 50 GHz. A similar level of mode coupling (-100 dB at 14 GHz to -62 dB at 50 GHz) between TE\(_{10}\) and TE\(_{20}\) modes is also observed for the substrate integrated waveguide case, as shown in Fig. 5.1(b). However, isolation between TE\(_{10}\) and TE\(_{30}\) is only between 20 dB and 50 dB from 14 GHz to 50 GHz. Overall, there seems to be no significant energy coupling from the fundamental mode to the higher order modes in the waveguide. This suggests the possibility of using substrate integrated waveguides over an ultra-wide frequency range (36 GHz in this example).

To investigate lower frequency region of waveguide operation, the normalized phase constants of the TE\(_{10}\) mode of the substrate integrated waveguide and solid waveguide are generated in Fig. 5.2. The normalized phase constant of an ideal TEM line is included in the same figure. Fullwave simulations show that the phase constant \(\beta\) of the two waveguides
5.2 Signal Integrity Analysis of the Waveguide Interconnect

![Graph](image1)

**Fig. 5.1** Fullwave simulations of coupling in $TE$ modes of a: (a) solid waveguide. (b) substrate integrated waveguide.

are almost identical and become more linear at high frequencies, but at lower end strong dispersive characteristic is observed. Hence, when the baseband signal is upconverted to be transmitted through this bandpass channel, the region very close to the cutoff should be avoided.

![Graph](image2)

**Fig. 5.2** Comparison of normalized phase constant ($\beta/\beta_0$) in SIW, solid waveguide and ideal TEM transmission line.
5.3 A Digital Signaling System Using Waveguide Interconnects

Digital transmission through a bandpass channel imposes new requirements to the design of driver and receiver stages. To accommodate for baseband transmission, these blocks should contain mixers for up-conversion and down-conversion of digital signals, as shown in Fig. 5.3. In addition, a lowpass filter is used to remove unwanted images resulting from the down-conversion process. In order to design such a system, the following steps are suggested.

1. The highest rate of data transmission is chosen, and, hence, the required signal bandwidth ($B_{\text{signal}}$) can be estimated.

2. Next, the mixer specifications can be determined. Its IF bandwidth is dictated by the signal bandwidth. The frequency range of modulation, which is found to be between $f_{\text{LO}} - B_{\text{signal}}$ and $f_{\text{LO}} + B_{\text{signal}}$, determines the required RF bandwidth of the mixer. $f_{\text{LO}}$ is the required local oscillator frequency that must fall within the LO bandwidth of the mixer.

3. The width of the waveguide is then chosen by knowing the modulation frequency band and the substrate type.

4. The undesired image signal resulting from the down-conversion has the center frequency corresponding to $2f_{\text{LO}}$. Therefore, the stopband region of the lowpass filter should have significant attenuation well below $2f_{\text{LO}} - B_{\text{signal}}$. In addition, the passband of the filter must also accommodate the required $B_{\text{signal}}$ bandwidth.

![Fig. 5.3 A waveguide interconnect system for digital data transmission.](image-url)
For the rest of this section, complete description of a waveguide interconnect system will be presented. To enable high-speed data transmission, optimized system architecture and component specifications are also explained herein.

### 5.3.1 Digital Source

To demonstrate operation of the system in a practical application, transmission rate of 3.125 Gb/s was chosen. This rate corresponds to the maximum line rate on the XAUI standard that is used in many backplane applications and other 10G interfaces [18]. The typical 10–90% risetime ($\tau_r$) of an Anritsu MP1763C pulse pattern generator used in this work is reported to be 30 ps. Thus, for the data rate of interest, the maximum signal bandwidth ($0.8/\pi \tau_r$) is estimated to be 8.49 GHz [107]. A nominal signal bandwidth of 8 GHz ($B_{signal}$) is therefore considered to be sufficient for transmission of significant components of the pulse.

### 5.3.2 Driver and Receiver Stages

From the required $B_{signal}$, it is estimated that the IF bandwidth of the mixer should be around 8 GHz. In order to keep the size of the waveguide as small as possible, the $f_{LO}$ is chosen to be around 20 GHz. Effectively, the required RF bandwidth is between 12–28 GHz. Hence, the closest available off-the-shelf mixer is a Marki Microwave double-balanced M1R-0726 mixer with RF/LO bandwidth of 7–26.5 GHz and IF bandwidth of DC–8 GHz. The conversion loss of this mixer is between 6 dB to 7 dB according to the supplier’s datasheet. The same type of mixer will also be used in the receiver stage where the RF signal is demodulated and the baseband waveform is recovered by using a lowpass filter.

In this scenario, the undesired image signal resulting from the receiver mixer will have the center frequency corresponding to around 40 GHz. For a signal bandwidth of 8 GHz, the stopband of the lowpass filter should start much earlier than 32 GHz. Additionally, the bandwidth of the lowpass filter should be close to 8 GHz in order not to significantly distort the received signal. A Mini-Circuit VLF-6700 lowpass filter with the 3-dB cutoff frequency of 7.6 GHz has the closest specification to our system requirements. The insertion loss of the filter is higher than 20 dB at 9.3 GHz and beyond, which provides adequate suppression of the unwanted signals.
5.3.3 Waveguide Prototype

To ensure availability of sufficient transmission bandwidth for the chosen data rate, the overall bandwidth of the waveguide interconnect is chosen to be wide enough to transmit pulses with the maximum bandwidth of 14 GHz with the lowest possible dispersion. Therefore, the cutoff frequencies of 14 GHz and 28 GHz were chosen for TE\(_{10}\) and TE\(_{20}\) modes, respectively. Rogers RO3006 was used as the substrate for implementation of the waveguide, having \(\epsilon_r = 6.15\) and \(\tan\delta = 0.0020\) measured at 10 GHz. Lower transmission losses are expected in comparison with FR4-based waveguides. The coplanar microstrip-to-waveguide transition, which is essentially a tapered microstrip line as explained in Section 3.7.1, is chosen to feed the waveguide. The 50-\(\Omega\) microstrip line has a width of 0.9 mm. For the chosen waveguide width of 4.1286 mm, the width and length of the coplanar transitions are 2.2 mm and 2 mm, respectively. Its total length is 49 mm, which includes the transition sections.

The waveguide prototype inserted in a 3680K Wiltron universal test fixture is shown in Fig. 5.4(a). The test fixture provides a better contact and lower parasitics compared to the soldered connectors. As discussed earlier, the waveguide bandwidth extends beyond the single mode region. Fig. 5.4(b) depicts the measured transmission coefficient of the waveguide TE\(_{10}\) mode with the bandwidth of at least 19 GHz, measured at 3 dB below the maximum. The cutoff frequency is around 14 GHz and a minimum insertion loss of 2.44 dB is obtained. For comparison, magnitude of the \(S_{21}\)-parameter derived from an FEM solver is also presented in the same figure. In the cutoff region, the magnitude of the simulated \(S_{21}\)-parameter is much lower than that of the measurement due to the larger dynamic range provided by the fullwave solver. It can be observed that the waveguide passband obtained from the simulation is much more flat and less attenuated. The difference in the measured and simulated results can be attributed to the test fixture, which is not included in the fullwave model. Finally, the specifications of mixers, lowpass filter, and waveguide used in this waveguide interconnect system are summarized in Table 5.1.

5.4 High-speed Data Transmission

In this section, the waveguide-based interconnect system described in Section 5.3 is experimentally evaluated for high-speed data transmission. The measurement setup of the
5.4 High-speed Data Transmission

![Image of SIW prototype and measured simulated S21 parameters](image)

**Fig. 5.4**  (a) Fabricated SIW prototype in a Rogers RO3006 substrate situated on a 3680K Wiltron universal test fixture. (b) Measured and simulated $S_{21}$-parameters.

**Table 5.1** Waveguide Interconnect System Components Specifications

<table>
<thead>
<tr>
<th>Components</th>
<th>Specifications</th>
</tr>
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<tbody>
<tr>
<td>Mixer (datasheet)</td>
<td>IF BW: DC–8 GHz</td>
</tr>
<tr>
<td></td>
<td>RF BW: 7–26.5GHz</td>
</tr>
<tr>
<td>LP Filter (datasheet)</td>
<td>3-dB Cutoff: 7.6 GHz</td>
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<td>20-dB Cutoff: 9.3 GHz</td>
</tr>
<tr>
<td>Waveguide (measured)</td>
<td>3-dB BW: 15.3–34.5 GHz</td>
</tr>
</tbody>
</table>

A high-speed system is presented in Fig. 5.5. To derive the data transmission system, an Anritsu MP1763C pattern generator with an external trigger, which can provide up to 12.5-Gb/s of pseudo-random binary sequence (PRBS), is employed. A Tektronix TDS8200 digital sampling oscilloscope with 80E06 70-GHz sampling module is used to monitor the output eye diagrams.

Since both mixers need to be synchronized, the LO of the two mixers are derived by an Anritsu MG3696B signal generator through an Agilent 11636B resistive power divider. The power divider has a typical insertion loss of 7.5 dB in the operation bandwidth of DC to 26.5 GHz. At frequencies above 20 GHz, the signal generator can supply no more than 10 dBm of leveled output power. Due to an extra loss through the resistive power divider, two Agilent 83051A amplifiers are used to drive each of the mixers to ensure sufficient LO power to turn on the mixers. The amplifier has the following specifications: bandwidth =
High-Speed Data Transmission in Waveguide-based Interconnects

Fig. 5.5  Measurement setup of a waveguide interconnect system.

0.045–50 GHz, $G_{\text{min}} = 23$ dB (minimum gain), and $P_{\text{sat, min}} = 12$ dBm (minimum saturation power). The picture of the described system is shown in Fig. 5.6.

Fig. 5.6  Photograph of the system described in Fig. 5.5.

5.4.1 Demonstrating System Operation at 3.125 Gb/s

The output eye pattern is used as the indicator for the quality of signal transmission. As practiced in digital engineering, a large eye opening is desirable in order to avoid detection
errors. Parameters, such as eye height, eye width and jitter, are often inspected to determine
the eye quality [108, 109]. Eye height dictates the amount of noise margin that the system
can tolerate. Eye width is the time interval over which the waveform can be uniformly
sampled without decision errors [109]. Finally, jitter is the time-base variation of the pulse
from its ideal location, which causes a reduction in the timing margins. The ideal location
can be defined as the delayed version of the input signal ignoring any system imperfections.
In this work, peak-to-peak jitter is measured at the threshold crossing, i.e., half of the eye
height. In common practice, an eye mask, which is specific to a signaling standard, is used
to assess the overall quality of an eye pattern.

A nonreturn-to-zero (NRZ) pulse with amplitude of 250 mV\textsubscript{p-p} supplied by the pattern
generator is the input signal to the driver mixer. The measured output eye diagram by
the digitizing oscilloscope is presented in Fig. 5.7(a). The LO frequency was adjusted to
be 21.6 GHz for the best output waveform, which also utilizes the less dispersive frequency
region of waveguide operation (see Fig. 5.2). Measured peak-to-peak amplitude, eye height,
eye width, rise/fall times and peak-to-peak jitter are summarized in Table 5.2. It can be
observed that the eye height is about one-quarter of the input, which is mainly due to the
nominal 6-dB conversion loss incurring in each mixer. Nonetheless, the output waveform
has a clear pulse shape and the eye opening is relatively wide.

The output eye height of the waveguide interconnect system can be predicted using the
system loss calculation of a typical binary phase shift keying (BPSK) modulation system.
Derivation of the expression is described herein. Consider the following functions:

- Input digital signal, \(d(t)\)
- Carrier wave at the LO of the input mixer, \(c_1(t)\)
- Carrier wave at the LO of the output mixer, \(c_2(t)\)

Carrier \(c_1(t)\) with amplitude \(A_{c_1}\) and frequency \(f_{LO}\) is expressed by the following cosine
function:

\[
c_1(t) = A_{c_1} \cos(2\pi f_{LO} t).
\]  

(5.1)

Carrier \(c_2(t)\) also follows the same characteristic with a phase shift, \(\phi\), as defined below.

\[
c_2(t) = A_{c_2} \cos(2\pi f_{LO} t + \phi).
\]  

(5.2)
It is assumed that the input and output mixers have conversion gains of $G_1$ and $G_2$, respectively, which are constant over the operation frequency range. The modulated signal can be expressed as:

$$m(t) = G_1 d(t)c_1(t) = A_{c1}G_1 \cos(2\pi f_{LO}t)d(t). \quad (5.3)$$

Next, the Fourier Transform (FT) of the modulated signal in (5.3) is found to be:

$$M(f) = \frac{1}{2}A_{c1}G_1[D(f - f_{LO}) + D(f + f_{LO})]. \quad (5.4)$$

where $d(t) \rightarrow D(f)$, $m(t) \rightarrow M(f)$, and $\rightarrow$ indicates the Fourier transform. This implies that the spectrum of the baseband signal, $d(t)$, is shifted to $+f_{LO}$ and $-f_{LO}$. When the modulated signal, $m(t)$, travels through an interconnect, it convolves with the impulse response of the interconnect, $h(t) \equiv H(f)$. Subsequently, the output of the receiver mixer is passed through a lowpass filter, $x(t) \equiv X(f)$, whose cutoff frequency is higher than the signal bandwidth ($B_{signal}$) but below $2f_{LO} - B_{signal}$. Therefore, the recovered digital signal is:

$$D'(f) = \frac{1}{2}A_{c1}A_{c2}G_1G_2\cos(\phi)H(f)D(f)X(f). \quad (5.5)$$

It should be noted that this analysis is employed to estimate the eye height measured at the center of the eye diagram. An example of the system loss calculation can be illustrated by considering the losses at the LO frequency of 21.6 GHz, which carries the DC component of the baseband signal. The transmission loss occurs in three installments: 5.5 dB (in up-conversion), 2.64 dB (in the SIW and its transitions), and 5.5 dB (in down-conversion). The mixer conversion loss is quoted from the manufacturer’s datasheet (typical value at 21.6 GHz). The output amplitude of the system can be approximated by equation (5.5). The input power of the mixer LO port is measured to be 13.5 dBm ($\approx 1.496 \text{ V}_{p-p}$), and both LO signals are approximately in-phase. The insertion loss of the filter is negligible around DC. Therefore, for a 250-mV input waveform, the expected output eye height is $58.20 \text{ mV} \times (250 \times 10^{-11.86dB/20})$, which is very close to the measured values in Table 5.2.

The output eye diagram can also be predicted from system simulations using circuit simulators such as Ansoft Designer [110]. The measured S-parameter network of the waveguide prototype and specifications of system components in Table 5.1 are incorporated in a
simulation test-bench, and the resulting output is presented in Fig. 5.7(b). The simulated eye height is found to be 7.9 mV smaller than that of the measured value. The eye height and peak-to-peak jitter are calculated to be 306.89 ps and 13.27 ps, respectively. Since some parameters in the models of the mixers and filter used in the circuit simulator assume constant characteristics, small discrepancies between the simulated and measured results are observed. Overall, the system simulation appears to predict the output eye diagram reasonably well.

To further investigate the measured output eye diagram, other experiments are conducted, first to determine amount of rise/fall time degradation and second to measure the bit error ratio. The output rise/fall times are degraded from 27/20 ps to 126/126 ps. This is due to the limited bandwidth of system components and transitions and mainly the lowpass filter at the output of the receiver mixer. This was determined by connecting the lowpass filter directly to the pattern generator and measuring the rise/fall times of the filter output. This test showed that the filter increased the output rise/fall times to 76/74 ps, as shown in Fig. 5.8. The peak-to-peak jitter of the 3.125-Gb/s NRZ pulse is slightly changed (11.2 ps). The overall filtering effects, dispersion and system losses also contribute to the increasing of the output peak-to-peak jitter from 4.2 ps to 30.8 ps.

In further evaluation of the output eye quality, an Anritsu MP1764C error detector was used to measure bit error ratio (BER). After a few minutes of transmitting PRBS patterns through the waveguide interconnect system, BER of less than $10^{-13}$ was obtained. Generally, a reliable high-speed system should be able to demonstrate BER better than $10^{-12}$ [53].

### 5.4.2 Operating the System at 5 Gb/s

Next, the system performance is inspected at faster data rates. The goal is to determine the maximum transmission capacity of the system without changing system components. In fact, components, such as mixers, lowpass filter and waveguide, are pushed to their bandwidth limits, as the data rate increases. Therefore, utilizing wideband driver and receiver stages is as crucial as allocating sufficient waveguide bandwidth to accommodate faster transmission rates. To demonstrate the system capability in transmission of higher speed data, a PRBS signal with 5 Gb/s data rate is applied to the waveguide-based interconnect system. The corresponding measured output eye diagram is presented in Fig. 5.9(a).
Fig. 5.7  Output eye diagrams of the waveguide interconnect system at 3.125 Gb/s. (a) Measured. (b) Simulated.

The respective eye parameters are also summarized in Table 5.2. The output eye height is decreased from 235.73 mV to 62.58 mV. There is also 22.18 ps reduction in the output eye width (11.1%). As well, the rise/fall times are degraded from 27/22 ps to 104/100 ps, and the peak-to-peak jitter is increased from 7.2 ps to 32.8 ps. The simulated output eye diagram as depicted in Fig. 5.9(b) shows a good agreement with the measured result. The simulated eye height, eye width and jitter are found to be 47.41 mV, 183.99 ps and 14.72 ps, respectively. Again, in order to evaluate the measured degradation of rise/fall times, the lowpass filter is placed right after the source and the eye diagram is measured at the filter output (see Fig. 5.10). It can be observed that the rise/fall times and peak-to-peak jitter of the PRBS signal are increased to 92/91 ps and 14.4 ps, respectively. As well, a bit error tester was connected to the output, and a BER of smaller than $10^{-13}$ was measured.

Overall, from the measurement results, it can be seen that a very good eye opening is still obtainable at this high-speed data rate with measured BER better than $10^{-13}$. However, when the data rate is increased beyond 7 Gb/s, the output eye opening closes. It was not possible to demonstrate the system performance for such high bit rates with the existing system components. Nonetheless, this experiment demonstrates the capability of an alternative interconnect system to support the emerging high-speed serial I/O standards.
5.5 Summary

A substrate integrated waveguide is a wideband transmission medium whose bandwidth is shown to extend beyond the TE$_{20}$ cutoff frequency. Thus, it is suitable for high-speed signaling. However, a waveguide-based interconnect is inherently a bandpass channel, which cannot be used to transmit baseband signals directly. Therefore, a system arrangement with specific requirements for the driver and receiver stages is proposed to overcome this challenge. Mixers are employed in the system for up-conversion and down-conversion of the baseband signals. A lowpass filter is also incorporated in the receiver section to recover baseband signals.

An SIW prototype was fabricated and evaluated experimentally. From the frequency-domain characterization, the 3-dB bandwidth of the waveguide prototype is measured to be at least 19 GHz. Furthermore, the fabricated waveguide is incorporated in the system for high-speed signal transmission measurement. It is demonstrated experimentally that the waveguide-based interconnect system is capable of delivering high-speed data of up to 5 Gb/s with very clean eye diagrams.
Fig. 5.8  Measured 3.125 Gb/s PRBS source after filtering.

Fig. 5.9  Output eye diagrams of the waveguide interconnect system at 5 Gb/s. (a) Measured. (b) Simulated.
Table 5.2  Measured Output Eye Diagrams of the Waveguide-based Interconnect System (Figs. 5.7(a) and 5.9(a))

<table>
<thead>
<tr>
<th></th>
<th>3.125 Gb/s</th>
<th></th>
<th>5 Gb/s</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Source</td>
<td>Output</td>
<td>Source</td>
<td>Output</td>
</tr>
<tr>
<td>$V_{p-p}$ (mV)</td>
<td>284</td>
<td>113</td>
<td>289</td>
<td>114</td>
</tr>
<tr>
<td>Eye Height (mV)</td>
<td>233.75</td>
<td>61.67</td>
<td>235.73</td>
<td>62.58</td>
</tr>
<tr>
<td>Eye Width (ps)</td>
<td>314.62</td>
<td>293.84</td>
<td>194.38</td>
<td>172.20</td>
</tr>
<tr>
<td>Rise Time (ps)</td>
<td>27</td>
<td>126</td>
<td>27</td>
<td>104</td>
</tr>
<tr>
<td>Fall Time (ps)</td>
<td>20</td>
<td>126</td>
<td>22</td>
<td>100</td>
</tr>
<tr>
<td>Pk-pk Jitter (ps)</td>
<td>4.2</td>
<td>30.8</td>
<td>7.2</td>
<td>32.8</td>
</tr>
</tbody>
</table>

Fig. 5.10  Measured 5 Gb/s PRBS source after filtering.
Chapter 6

Hybrid Substrate Integrated Waveguide

6.1 Introduction

In the previous chapters, it was demonstrated that the waveguide interconnect provides excellent quality of transmission for high-speed digital signals. Furthermore, it exhibits low losses and excellent immunity to crosstalk and EMI. The width of the substrate integrated waveguide is determined by the frequency range of operation. In tens of gigahertz frequency range, the waveguide width is still relatively large compared to that of a microstrip or stripline. This constraints usage of the waveguides in a compact integration platform. Common printed circuit boards and backplane use substrate materials with lower dielectric constants compared to the case discussed in Section 5.3. For example, if FR4 was used as the base substrate in that discussion, the waveguide width would have increased from 4.13 mm to 5 mm. To compensate for the relatively larger volume occupied by the waveguide, a hybrid or dual-mode transmission channel is introduced in this chapter by routing striplines inside the waveguide. In Section 6.2, the hybrid SIW structure is described. In Section 6.3, the hybrid structures are characterized from the signal integrity point of view. The needed transition geometries for routing the striplines in and out of the waveguide are described in Section 6.4. In Section 6.5, the hybrid prototypes with single and two embedded striplines are fabricated and tested by high-speed system measurements. A comparative study using system simulations is presented in Section 6.6 to demonstrate the ultra-high-speed trans-
mission capacity of the proposed hybrid waveguide-based interconnect system.

6.2 Hybrid Substrate Integrated Waveguide Structure

A hybrid substrate integrated waveguide as shown in Fig. 6.1 is formed by inserting a number of striplines inside the waveguide volume. The side view of the hybrid structures discussed here is depicted in Fig. 6.1(c). The dual interconnect structure of Fig. 6.1(a), which has a single embedded stripline, has a unique characteristic in that it enables simultaneous signal propagation along the stripline and waveguide. In this manner, the waveguide volume is reutilized, and the transmitted data rate is doubled or tripled by channel reuse. In fact, here, a multimode transmission concept is employed, which ensures efficient propagation of uncorrelated modes, i.e., TEM and TE_{10}, in the same space. The electric field profiles of these fundamental propagating modes are different, and, to further ensure minimal mode coupling, the two interconnects are utilized in different frequency ranges. It will be shown in the subsequent sections that the impact of adding striplines on the signal propagation in the waveguide is insignificant, particularly, in terms of crosstalk between the two fundamental modes.

Typically, the ratio of stripline and waveguide widths can be as small as 1:10. Therefore, a few more striplines can be placed inside the waveguide to exploit the available substrate volume more efficiently and ultimately increase the interconnect density and aggregate transmission rate. The maximum number of striplines is determined by the crosstalk tolerance of the system and the minimum allowed spacing from the via sidewalls in the fabrication process. In this way, a hybrid SIW can be utilized more efficiently in terms of aggregate transmission capacity by employing more embedded striplines. A second hybrid SIW interconnect with two embedded striplines as shown in Fig. 6.1(b) will also be investigated in this chapter.

6.3 Characterization of Hybrid Structures from Signal Integrity Perspective

In the hybrid structure of Fig. 6.1(a), a stripline is embedded inside the SIW. Inspection of the characteristic impedance ($Z_o$) of the stripline is important in signal integrity considerations. A fullwave simulator is used to observe the effect of the conducting sidewalls on
Fig. 6.1 Hybrid SIW structures. (a) Single embedded stripline. (b) Two embedded striplines. (c) Side view of both structures.
6.3 Characterization of Hybrid Structures from Signal Integrity Perspective

$Z_o$ of the stripline. The stripline is centered in the waveguide ($h_1 = h_2$), which is developed in a Rogers 4003C substrate ($\epsilon_r = 3.38$ and $\tan\delta = 0.0027$ measured at 10 GHz). It is noted that this substrate material is different from those used in Chapter 5 due to ease of multilayer PCB fabrication. The symmetric stripline has a width ($W$) of 0.54 mm in order to ideally obtain a characteristic impedance of 50 $\Omega$. Fig. 6.2 shows $Z_o$ of a stripline without any via sidewalls and that of the embedded stripline when $W_g$ is 3 mm and 5.8 mm. It is observed that there are no significant changes in $Z_o$ (less than 1%) when conducting sidewalls are placed closer to the stripline structure ($W_g = 3$ mm case). In general, our simulations showed that the estimations used in placing via fences near the striplines [97], i.e., $S/h > 1$, can be used here as well.

![Simulated characteristic impedance of the embedded stripline.](image)

Besides maintaining $Z_o$ of the stripline, mode coupling or, in another term, crosstalk, is the other important signal integrity concern. The profile of the fundamental propagating modes of the stripline and SIW are shown in Fig. 6.3. It is desirable that these modes are not coupled to each other. It can be observed from the figure that the two modes have different electric field distribution profile. Additionally, to further ensure minimal mode coupling, the two interconnects are utilized in different frequency ranges. Stripline is a lowpass interconnect whereas the waveguide is used in a higher frequency region.

To quantify this, fullwave analysis is used to evaluate coupling between the TEM and TE$_{10}$ modes of the structure in Fig. 6.1(a). In this study, the waveguide dimensions are chosen to be $a = 1$ mm, $D = 0.5714$ mm, $h = 0.915$ mm, and $W_g = 5.8$ mm, which yields the TE$_{10}$ cutoff frequency of 13.9 GHz on a Rogers 4003C substrate. A stripline is centered
in the waveguide, and has a width ($W$) of 0.54 mm in order to obtain a characteristic impedance of 50 Ω. The total length of the structure is 15 mm. Fig. 6.4(a) shows the mode coupling parameters. For instance, the plotted parameter, $S(2:\text{TE}_{10},1:\text{TEM})$, is a relative measure of $\text{TE}_{10}$ energy detected at port 2 of the waveguide when port 1 is excited by a TEM wave. It can be observed that mode couplings in this structure are almost negligible (less than -65 dB) as expected. When the via sidewalls are closer to the stripline, i.e., $W_g = 3$ mm, the mode coupling is still negligible, as shown by the isolation of more than 50 dB in Fig. 6.4(b).

Next, the hybrid structure with two striplines as shown in Fig. 6.1(b) is designed such that there is negligible coupling between the two embedded lines in order to simplify our
6.3 Characterization of Hybrid Structures from Signal Integrity Perspective

studies. The case of strong coupling and possibility of using differential signalling are not considered within the scope of the present work. The simulations prove that each of the stripline can be treated as an isolated (single-ended) transmission line with good accuracy. Therefore, the $Z_0$ characteristics shown in Fig. 6.2 also applies to the new hybrid structure. In these simulations, the two striplines have the spacing ($G$) of 1.9 mm. To investigate mode coupling when two striplines are embedded, it is considered that the minimum allowed isolation between the striplines is 20 dB. Fullwave simulations (not shown here for brevity) indicate that the near- and far-end crosstalks of the striplines are significantly lower than -20 dB. For analysis of coupling between TEM and TE$_{10}$ modes, one of the striplines is excited by the TEM mode, and the TE$_{10}$ mode energy is detected at the other end of the waveguide, and vice versa. The worst-case TEM-TE$_{10}$ coupling is presented in Fig. 6.5, as labeled by “Two Striplines”. The host waveguide is the same as the “One Stripline” case, which is derived from the worst-case coupling found in Fig. 6.4(a). It can be observed that still less than -65 dB coupling exists when the waveguide contains more than one stripline. This confirms the feasibility of increasing the interconnect density inside the hybrid structure.

![Fig. 6.5](image)

**Fig. 6.5** Simulated worst-case coupling between TEM and TE$_{10}$ modes when one and two striplines are embedded in the SIW for $W_g = 5.8$ mm.

It is expected that, as discontinuities appear in the hybrid structure due to stripline routing, mode coupling levels will increase. Therefore, this discussion is continued in the subsequent sections.
6.3.1 Hybrid Bend Geometry

In Section 3.5, the waveguide interconnect has been demonstrated to be very efficient in guiding signals around sharp corner. This assertion, in principle, should be applicable to the hybrid geometry. Fig. 6.6 shows an illustration of this routing scenario when one and two striplines are present in the waveguide.

![Fig. 6.6 Hybrid SIW bends containing: (a) Single embedded stripline. (b) Two embedded striplines.](image)

In order to verify the assumption, a fullwave analysis is performed for the hybrid SIW bend geometries shown in Fig. 6.6 when $W_g = 5.8$ mm. All other waveguide and stripline parameters are the same as those used earlier in this section. The equivalent length of each bend structure is measured to be 24.32 mm. The spacing between the embedded lines is 1.9 mm for the two-stripline case, which ensures very small coupling between them (54.5 dB and 37.5 dB for near- and far-end crosstalks, respectively, see Fig. 6.7). Transmission and coupling parameters of the waveguide section in the hybrid SIW are presented in Fig. 6.8. For comparison, another uniform hybrid SIW section having the same total length is also simulated, and the results are included in the same graph. From Fig. 6.8(a), it is observed that there is very small difference ($< 0.2$ dB) in the transmission coefficients of the straight and bend geometries over the 14–30 GHz frequency range, except at 27.5 GHz. The small
dip observed in the case of one embedded stripline can be attributed to the slight deviation in the cross-sectional width at the corner in which some TE$_{10}$ energy is coupled to the TE$_{20}$ mode. When two striplines are present, a shaper dip appears as the TE$_{20}$ mode excited by the bend discontinuity is easily coupled into both striplines. Nonetheless, the discontinuity introduced by the bend has no significant impact on the coupling between the TEM and TE$_{10}$ modes when comparing with the respective results from the uniform section, as shown in Fig. 6.8(b). This confirms the efficiency of the hybrid SIW bend routing configuration.

![Fig. 6.7](Image)

**Fig. 6.7** Coupling between two embedded striplines in the hybrid SIW bend geometry shown in Fig. 6.6(b).

### 6.4 Routing and Transition Design

To integrate the hybrid structure with other system components proper transition structures are needed. The coplanar microstrip-to-waveguide transition is chosen for connecting the waveguide to microstrip lines. Routing the striplines in and out of the waveguide should result in a minimal impact on the quality of signal transmission. For this purpose, two routing scenarios as shown in Fig. 6.9, *i.e.*, vertical-entry and side-entry, are suggested and investigated in this section.

In the vertical routing case presented in Fig. 6.9(a), a via transition is used to transfer signal from the microstrip (quasi-TEM mode) in the upper metal layer to the embedded stripline (TEM mode). The portion of the via that is inside the waveguide can also serve as the excitation source for the TE$_{10}$ mode. Therefore, part of the signal energy that was meant to be delivered to the stripline port (port 3) is transferred to the TE$_{10}$ mode of the
waveguide. This coupling can be minimized by placing the via away from the center of the waveguide, as indicated by the parameter called “Offset” in Fig. 6.9(a). The effect of changing the offset is presented in Fig. 6.10 by showing the transmission coefficients of the TE_{10} mode. It can be seen that the transmission performance of the waveguide mode improves as the via is placed away from the center of the waveguide, i.e., closer to a sidewall. This can be attributed to the fact that the TE_{10} electric field has a sinusoidal distribution (half-period sine wave) across the waveguide width. When the via is placed at the center, the coupling of the TE_{10} mode to the via is the greatest, as its magnitude is at maximum. On the contrary, the electric field strength of the TE_{10} mode decreases when moving away from the center of the waveguide in the lateral direction. Nonetheless, this type of transition is quite susceptible to mode coupling, as the TE_{10} wave can easily induce currents on the via. For instance, when the center of the via is 2 mm away from the center of the waveguide, the TEM-TE_{10} coupling level varies between 10–20 dB in the waveguide passband up to 30 GHz. Hence, this routing configuration may not be seen as the most efficient one.

An alternative method is to change the entry point to the waveguide sidewall, as depicted in Fig. 6.9(b). The side-entry transition is formed by creating an opening window of width S_w in the sidewall. In the design of the side-entry transition, two considerations have to be taken into account. First, the window width should be optimized to create a
Fig. 6.9 Possible routing scenarios for routing a stripline in and out of a SIW. (a) Vertical-entry. (b) Side-entry.
matching condition or minimum loading due to the discontinuity in the signal propagating on the stripline, i.e., the power loss due to the reflection at the entry point is minimized. Second, the leakage of the waveguide mode through the window has to be kept as low as possible. These constraints are investigated by fullwave simulations of the structure shown in Fig. 6.9(b). The dimensions of the stripline and waveguide are the same as those in Section 6.3. The total lengths of the waveguide and stripline are 22 mm and 27 mm, respectively. In this study, $S_w$ is varied between 0.65–2.25 mm while the transmission coefficient from port 2 to port 3 is monitored. From parametric simulations in Fig. 6.11(a), it can be observed that $S_w$ affects matching and signal transmission ($S_{32}$), especially at high frequencies. However, this range is well above the operation bandwidth of the stripline for baseband transmission. Fig. 6.11(b) also shows that $S_w$ must be chosen as small as possible in order to maximize the transmission coefficient of the TE$_{10}$ mode propagating along the waveguide ($S_{31}$). It can be observed that the entry window must be kept as small as possible to minimize the leakage of the waveguide TE$_{10}$ mode. Therefore, $S_w$ of 1.45 mm is chosen for optimum waveguide and stripline transmission characteristics. It is concluded that simultaneous two-channel transmission with excellent quality is achieved in the proposed scheme.

In addition, to test the channel isolation, port 3 is excited by TE$_{10}$ and TEM modes, respectively, and the transmission to the other ports is monitored. Fig. 6.12 depicts the simulated results of this mode coupling test. It can be observed that coupling to TEM mode (port 2) with TE$_{10}$ excitation is less than -74 dB, i.e., $S(2:\text{TEM},3:\text{TE}_{10})$, in a 30-
GHz frequency range. Additionally, isolation between ports 1 and 2 (or 3) is excellent (more than 75 dB). This can be seen in the coupling from TEM mode to TE_{10} mode (port 1), i.e., S(1:TE_{10}, 2:TEM) and S(1:TE_{10}, 3:TEM). Thus, high level of isolation between the modes is still attainable even in the presence of the side-entry transition.

![Figure 6.11](image1)

**(a)** Simulated transmission coefficients of the structure in Fig. 6.9(b) for various window sizes (S_w). (a) Stripline. (b) SIW.

![Figure 6.12](image2)

**(b)** Simulated isolation parameters of the dual-mode structure in Fig. 6.9(b).

The side-entry transition is also employed for routing two striplines in and out of the waveguide, as shown in Fig. 6.13(a). Through fullwave simulations, S_w is optimized to achieve minimum reflection back to port 3 (or port 4 when the window in the other sidewall
is designed) and to prevent significant field leakage to the outside. Hence, $S_w = 1.45$ mm is found. After designing the two routing windows, fullwave analysis is performed to monitor mode coupling. Fig. 6.13(b) shows isolation between the TEM and TE$_{10}$ modes. For instance, in $S(1:\text{TE}_{10},2:\text{TEM})$, port 2 is excited by the TEM mode on stripline 1 when port 1 detects the received TE$_{10}$ energy. The observed non-symmetric behavior is attributed to the numerical errors when the coupling values are less than -70 dB. Overall, it can be concluded that mode isolation is virtually unaffected, as it remains above 65 dB.

6.5 Experimental Evaluation of the Hybrid SIW Prototypes

6.5.1 Single Embedded Stripline

Fig. 6.14(a) shows the hybrid interconnect system in which microstrip line ports are used to feed the waveguide and embedded stripline. The waveguide is connected to a microstrip by using a coplanar microstrip-to-waveguide transition whereas the stripline is routed through a via hole to a microstrip line in the top metal layer. Due to the existence of this microstrip-via-stripline transition, the isolation between port 1 and port 2 is degraded, as the parallel-plate waveguide (PPW) mode can be excited by the via hole. A fullwave simulator is used to monitor the coupling between the three ports and different transmission modes. For example, port 2 is excited by the quasi-TEM mode and the quasi-TEM mode is measured at the other microstrip end, i.e., port 1. This yields the $S(1:Q\text{-TEM},2:Q\text{-TEM})$ as shown in Fig. 6.14(b). It is observed that isolation between ports 1 and 2 is degraded compared to that of Fig. 6.12. When port 2 is excited, the via discontinuity couples part of the signal energy into the substrate and hence to port 1. The same mechanism also applies when port 3 is excited by the TEM mode, as labeled by $S(1:Q\text{-TEM},3:\text{TEM})$ in Fig. 6.14(b). This phenomenon is confirmed by observing the electric field distributions at 9.4 GHz, as presented in Fig. 6.15, where the coupling to the substrate through the via transition is the strongest. When port 3 is excited by TE$_{10}$ mode and quasi-TEM mode is measured at port 2, i.e., $S(2:Q\text{-TEM},3:TE_{10})$ in Fig. 6.14(b), excellent isolation is obtained below the waveguide cutoff frequency. However, beyond 14 GHz, the coupling from TE$_{10}$ into port 2 is noticeably increased but still lower than -30 dB. This can be attributed to the TE$_{10}$ mode leakage through the entry window. The leaked energy propagates in the parallel-plate section and eventually couples to the via transition. Overall, the achieved isolation value is
Fig. 6.13  (a) Hybrid SIW with the side-entry transitions. (b) Simulated mode coupling parameters.
quite acceptable (better than 30 dB), except in the frequency range of 8.6–11.1 GHz where it is between 22 dB and 30 dB.

Fig. 6.14  Possible implementation of the hybrid SIW structure. (a) Geometry. (b) Coupling coefficients.

In order to demonstrate the dual-mode transmission concept experimentally, a 48-mm long prototype as shown in Fig. 6.16 was fabricated on a Rogers 4003C substrate by using a multilayer PCB manufacturing process. The total substrate thickness is 0.915 mm. The vertical profile contains three 0.305-mm thick dielectric layers for routing striplines and microstrip lines. Due to fabrication considerations, the stripline is an offset-type whose superstrate and substrate thicknesses are 0.610 mm ($h_1$) and 0.305 mm ($h_2$), respectively; see Fig. 6.1(c). The stripline has a width of 0.45 mm to obtain a 50-Ω characteristic impedance. The side-entry transitions are used to route the stripline in and out of the waveguide. In order to inject signal into the stripline from the top layer of the board, a microstrip-to-stripline via transition is employed. The waveguide has $W_g$ of 5.8 mm to obtain the TE$_{10}$ cutoff frequency of 13.9 GHz similar to the waveguide prototype in Section 5.3. This allows utilizing the same system setup. The other waveguide dimensions are the same as the one described in Section 6.3.

Next, the test structure is inserted in the universal test fixture, and characterized by S-parameter measurements using SOLT calibration technique. Since the prototype is a 4-port device, the unused ports are terminated to broadband 50-Ω loads in each 2-port measurement. The transmission coefficients of the waveguide and stripline are depicted
in Fig. 6.17. It can be observed that the waveguide has a good measured transmission characteristic with minimum insertion loss of 2.65 dB and wide 3-dB bandwidth of 18.74 GHz (between 13.65–32.39 GHz). Fullwave simulations of the test structure are performed and presented in the same figure. The sidewalls are, however, approximated by solid conductor walls in order to reduce the computational size. The connector models, which are derived from their structural layouts, are also included in the simulations. There are some discrepancies between the simulations and measurements, which can be attributed to fabrication errors and the discontinuities between the board and test ports. As well, the test fixture is not included in the layout simulations. Overall, the measured characteristics are very comparable to those of the waveguide prototype in Section 5.3.3. However, in this case, the 3-dB bandwidth is decreased by 4 GHz due to fabrication errors and the additional discontinuities. For the stripline, its bandwidth only extends up to 6.6 GHz. The reduction in bandwidth and sharp resonances are due to the filtering and parasitic effects caused by the discontinuities between the board and SMA connectors and the microstrip-to-stripline
via transitions since it was not observed in the fullwave simulation of the embedded stripline when these effects were not included. The isolation between the waveguide and stripline modes are also monitored by simulations and measurements, as presented in Fig. 6.18. It can be observed that isolation of close to 20 dB or more is measured between ports 1–2 and 1–3 (note port labels in Fig. 6.16). In general, a good agreement between the simulated and measured isolation parameters is observed.

The system used for sending data in the waveguide section of the hybrid test structure of Fig. 6.16 is the same setup described in Section 5.3 (shown in Fig. 5.5). To excite the stripline interconnect, another output port of the pattern generator is connected to port 2 of the prototype in Fig. 6.16. The overall test setup is shown in Fig. 6.19. The output at port 3 is monitored by the same high-speed digital oscilloscope using 80E02 electrical module (bandwidth of 12.5 GHz). The 80E06 module (bandwidth of 70 GHz) is used for the waveguide system output. A 3.125-Gb/s NRZ pulse with an amplitude of 250 mV$_{p-p}$ is applied to the input of the stripline structure. Due to the system losses discussed in Section 5.4, it is expected that the amplitude of the output signal of the waveguide to be smaller than that of the stripline. In order to observe similar amplitude levels at both
outputs, the input to the waveguide system is increased to 500 mV$_{p-p}$. The DC component of the baseband signal is expected to experience these losses at the LO frequency of 21.6 GHz: 5.5 dB (in up-conversion), 3.75 dB (in the SIW), and 5.5 dB (in down-conversion). The mixer conversion loss is quoted from the manufacturer’s datasheet (typical value at 21.6 GHz). The input power of the mixer LO port is measured to be 13.5 dBm ($\approx 1.496$ V$_{p-p}$), and both LO signals are approximately in-phase. The insertion loss of the filter is negligible around DC. Therefore, from (5.5) in Section 5.4.1, for a 500-mV waveform, the expected output eye height is 102.4 mV ($500 \times 10^{-13.77 dB/20}$). Again, the predicted value is shown to be very close to the measured values found in Tables 6.1 and 6.2.

The output eye diagrams of both interconnects are observed simultaneously, as depicted in Fig. 6.20. In general, it can be seen that both output eye diagrams are quite clean. Although, the output eye of the stripline is slightly distorted, as its transmission performance is degraded by the filtering effects of the connectors, junctions and via transitions. The output eye parameters from the stripline and waveguide system are summarized in Table 6.1. From examining Table 6.1 data it can be seen that both outputs have comparable eye qualities. The eye height of the waveguide output is slightly lower (by 25.76 mV) than that of the stripline. In fact, the eye height of the waveguide (101.32 mV) is very close to the predicted value (102.4 mV) calculated earlier. The waveguide system output can be increased further by raising the amplitude of the input NRZ signal. This is, however, limited
by the input compression level of the driver mixer (5 dBm for this mixer). Alternatively, an application specific amplifier can be designed to increase the output level but it is out of the scope of this study. The eye width of the stripline output (295.60 ps) is very close to that of the waveguide system output (298.32 ps). Noticeable degradation in rise/fall times of both output pulses are observed. The rise/fall times of the waveguide output are 105/99 ps due to the reasons discussed in Section 5.4. The rise/fall times of the stripline output are increased to 78/88 ps mainly because of the lowpass filtering effects. The peak-to-peak jitter of the waveguide output is 5.6 ps larger than that of the stripline, which is partly caused by the limited bandwidth of the mixers.

Subsequently, the bit rate of the pattern generator is increased to 5 Gb/s with other
Fig. 6.20 Dual-mode system outputs: waveguide-based interconnect (top) and stripline (bottom) at 3.125 Gb/s.

Table 6.1 Measured Output Eye Diagram of the Hybrid Transmission System at 3.125 Gb/s (Fig. 6.20)

<table>
<thead>
<tr>
<th>Specifications</th>
<th>Source</th>
<th>Stripline Output</th>
<th>SIW Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{p-p}$ (mV)</td>
<td>284</td>
<td>265</td>
<td>175</td>
</tr>
<tr>
<td>Eye Height (mV)</td>
<td>233.75</td>
<td>127.08</td>
<td>101.32</td>
</tr>
<tr>
<td>Eye Width (ps)</td>
<td>314.62</td>
<td>295.60</td>
<td>298.23</td>
</tr>
<tr>
<td>Rise Time (ps)</td>
<td>27</td>
<td>78</td>
<td>105</td>
</tr>
<tr>
<td>Fall Time (ps)</td>
<td>20</td>
<td>88</td>
<td>99</td>
</tr>
<tr>
<td>Pk-pk Jitter (ps)</td>
<td>4.2</td>
<td>19.6</td>
<td>25.2</td>
</tr>
</tbody>
</table>

parameters remaining the same as the previous experiment. The waveguide and stripline output eye diagrams are monitored simultaneously as presented in Fig. 6.21. Again, it can be observed that both output eye diagrams are still quite clean at this high data rate. The pertinent eye diagram parameters are summarized in Table 6.2. The eye height of the waveguide and stripline outputs are 110.23 mV and 151.27 mV, respectively. The eye width of the waveguide output is 13.07 ps smaller than the that of the stripline output. The rise/fall times of the waveguide and stripline outputs are increased to 100/104 ps and 85/90 ps, respectively. The peak-to-peak jitter of the waveguide is 17.2 ps higher compared to the stripline output. This experiment demonstrates a promising approach in doubling data transmission rate in a waveguide-based interconnect by reusing the waveguide volume
and achieving 10 Gb/s transmission.

![Image of eye diagram]

**Fig. 6.21** Dual-mode system outputs: waveguide-based interconnect (top) and stripline (bottom) at 5Gb/s.

**Table 6.2** Measured Output Eye Diagram of the Hybrid Transmission System at 5 Gb/s (Fig. 6.21)

<table>
<thead>
<tr>
<th>Specifications</th>
<th>Source</th>
<th>Stripline Output</th>
<th>SIW Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{p-p}$ (mV)</td>
<td>289</td>
<td>279</td>
<td>185</td>
</tr>
<tr>
<td>Eye Height (mV)</td>
<td>235.73</td>
<td>151.27</td>
<td>110.23</td>
</tr>
<tr>
<td>Eye Width (ps)</td>
<td>194.38</td>
<td>178.78</td>
<td>165.71</td>
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<td>Rise Time (ps)</td>
<td>27</td>
<td>85</td>
<td>100</td>
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<tr>
<td>Fall Time (ps)</td>
<td>22</td>
<td>90</td>
<td>104</td>
</tr>
<tr>
<td>Pk-pk Jitter (ps)</td>
<td>7.2</td>
<td>19.6</td>
<td>36.8</td>
</tr>
</tbody>
</table>

In comparison with the results shown in Table 5.2 of Chapter 5, the measured eye height of the hybrid waveguide prototype (if 250-mV input is considered) at both data rates is between 7–11 mV smaller. This is expected as the insertion loss of this hybrid waveguide prototype at the LO frequency is 1.11 dB higher than that of Fig. 5.4. At 3.125-Gb/s data rate, the peak-to-peak jitter and eye width of the hybrid structure are slightly better than the previous case. This is partly due to the fact that the $\text{TE}_{10}$ cutoff frequency of the hybrid waveguide is almost 1 GHz lower than that of the waveguide prototype in Section 5.3.3. Effectively, the bandwidth of the lower side-band (with respect to the LO
frequency) is extended, and, hence, data-dependent jitter is slightly improved. For the timing performance at 5 Gb/s, the peak-to-peak jitter of the hybrid structure is measured slightly larger than that of the waveguide prototype in Chapter 5. This can be attributed to the larger roll off in the transmission characteristic of the hybrid prototype.

6.5.2 Increasing Aggregate Transmission Rate with Two Embedded Striplines

Another hybrid waveguide prototype as shown in Fig. 6.22, which contains two embedded striplines, is used to demonstrate higher aggregate transmission capacity. The 48-mm long waveguide prototype is fabricated with a Rogers 4003C substrate having the same dimensions ($W_g$ of 5.8 mm) as the SIW described earlier in Section 6.5.1. The spacing between the striplines is 1.9 mm. The side-entry transitions are used to route two striplines in and out of the waveguide.

![Diagram of the hybrid SIW prototype.](image)

VNA measurements and fullwave simulations were used to characterize this hybrid prototype. As shown in Fig. 6.23, the waveguide has a minimum insertion loss of 2.3 dB and its 3-dB bandwidth extends from 14.26 GHz to 32.38 GHz (only 0.62 GHz different from the single-stripline case). The 3-dB bandwidth of the stripline including the microstrip and
via sections was measured to be 6.8 GHz from insertion loss between ports 1 and 2. Similar results are also obtained for the other stripline link between ports 3 and 4. It is noted in Fig. 6.23(b) that a resonance behavior appears around 9 GHz in both simulated and measured results of stripline links which is attributed to microstrip-to-stripline via transition. From measurements, the near- and far-end crosstalks between the striplines were found to be less than -20 dB (not shown here for brevity). In the fullwave simulations, the sidewalls are again approximated by solid conductor walls in order to reduce the computational size. There are some discrepancies between the simulations and measurements, which can be attributed to fabrication errors and junction discontinuities between the board and test ports.

![Graph](image)

Fig. 6.23 Measured transmission parameters of the hybrid SIW with two embedded striplines. (a) SIW ($S_{65}$). (b) Stripline ($S_{21}$).

For mode coupling analysis, the isolation between the waveguide and stripline modes are also monitored by simulations and measurements. Fig. 6.24 shows typical near- and far-end crosstalk measurements. The port notations are depicted in Fig. 6.22. In general, good agreement between the simulated and measured isolation parameters are observed. It can be seen that isolation of close to 20 dB or more is measured between ports 1 and 5, and ports 2 and 5. The coupling is higher than those predicted from simulations when the microstrip-via-stripline transitions are not present. This is because of the radiation of the via transition, which creates coupling to the microstrip port of the waveguide. Nonetheless, port isolation of higher than approximately 20 dB is achieved.
6.5 Experimental Evaluation of the Hybrid SIW Prototypes

For demonstration of very high-speed transmission through the hybrid structure shown in Fig. 6.22, the waveguide interconnect system shown in Fig. 6.19 is further developed to accommodate three data channels. The complete diagram of the system is presented in Fig. 6.25. The main components of the system are the same as the ones used in Fig. 5.5 with some operational adjustments as follows. The local oscillator (LO) port of each mixer is driven by 13.5 dBm of amplified single tone 22.2-GHz source provided by an Anritsu MG3696B signal generator. A 250 mV\text{p-p} pseudo-random binary sequence supplied by an Anritsu MP1763C pattern generator is applied to the input of the waveguide. The other output data port of the MP1763C (500 mV\text{p-p}) is divided into two similar pulses by a power divider whose outputs are applied to the two embedded striplines. As presented in Fig. 6.26, the outputs of the waveguide and striplines are simultaneously monitored by 80E06 (70-GHz bandwidth) and 80E04 (20-GHz bandwidth) electrical sampling modules of a Tektronix TDS8200 oscilloscope, respectively, at 3.125 Gb/s and 5 Gb/s data rates. It can be observed that excellent eye openings are obtained in the waveguide transmission. However, the eye heights are less than those of the stripline outputs mainly due to 6-dB conversion loss in each mixer. As for the stripline outputs, the outputs are more jittery and the quality of the eye diagrams are affected due to additional transitions and components such as the resistive power divider. The eye parameters from the output of the hybrid system are summarized in Table 6.3 (only one stripline output is shown here).
In comparison with the single-stripline case (when 250-mV input is considered), the difference in eye heights are almost insignificant (4.72 mV at 3.125 Gb/s and 1.79 mV at 5 Gb/s). In addition, the difference of less than 5 ps in the eye width is observed in both scenarios. The peak-to-peak jitter of the two-stripline case at 3.125 Gb/s is 8.4 ps greater than that of the single-stripline case. This may be attributed to additional parasitic effects from the custom-made fixture utilizing K-connectors compared to the test fixture employed in the previous case. For 5-Gb/s data rate, the difference in the peak-to-peak jitter is 2.4 ps, which is due to measurement errors.

![System data transmission setup for the hybrid SIW with two embedded striplines.](image)

**Fig. 6.25** System data transmission setup for the hybrid SIW with two embedded striplines.

![Hybrid SIW system output eye diagrams. (a) 3.125 Gb/s. (b) 5 Gb/s.](image)

**Fig. 6.26** Hybrid SIW system output eye diagrams. (a) 3.125 Gb/s. (b) 5 Gb/s.
6.6 Study of Transmission Capacity

In Section 6.5.2, the experimental validation of the hybrid prototype with two embedded striplines has demonstrated aggregate data transmission rate of 15 Gb/s (5 Gb/s for each individual channel). The maximum achievable transmission capacity of the hybrid waveguide prototype is limited by the bandwidth of the mixers and lowpass filter utilized at the driver and receiver sections. To investigate the capability of the waveguide prototype, its measured S-parameters as shown in Fig. 6.23 are used in Ansoft Designer system simulations, while other system components (mixers and lowpass filter) are assumed to be ideal. Fig. 6.27 shows the simulated eye diagrams at the output of the waveguide interconnect of the hybrid prototype (channel 2 in Fig. 6.25). It can be observed from Fig. 6.27(a) that excellent transmission quality is obtained at the data rate of 13 Gb/s. However, the degradation in the output eye quality is more noticeable at 21-Gb/s data rate, as seen in Fig. 6.27(b). Nonetheless, the output eye quality is still acceptable. Quantitatively, its eye height (around 250 mV) is more than 200 mV, which complies with the jitter template (the eye mask) of the XAUI interface standard [18]. Therefore, it is concluded that the maximum transmission capacity of this waveguide interconnect is around 21 Gb/s.

To determine the transmission capacity of the embedded stripline, the measured S-parameters of Fig. 6.23 is used in the system simulation. At 13-Gb/s data transmission, good quality output eye diagram is observed through this stripline prototype, as shown in Fig. 6.28(a). The eye height is found to be around 300 mV. Further simulations show that the transmission quality is drastically degraded in each of the stripline interconnects when the input data rate is increased. Beyond this data rate, output eye closure starts to

<table>
<thead>
<tr>
<th></th>
<th>Waveguide</th>
<th>Stripline</th>
<th>Waveguide</th>
<th>Stripline</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{p-p}$ (mV)</td>
<td>99</td>
<td>318</td>
<td>100</td>
<td>330</td>
</tr>
<tr>
<td>Eye Height (mV)</td>
<td>55.22</td>
<td>121.59</td>
<td>53.63</td>
<td>124.97</td>
</tr>
<tr>
<td>Eye Width (ps)</td>
<td>297.31</td>
<td>281.15</td>
<td>174.72</td>
<td>164.76</td>
</tr>
<tr>
<td>Rise Time (ps)</td>
<td>116</td>
<td>105</td>
<td>119</td>
<td>92</td>
</tr>
<tr>
<td>Fall Time (ps)</td>
<td>109</td>
<td>110</td>
<td>122</td>
<td>102</td>
</tr>
<tr>
<td>Pk-pk Jitter (ps)</td>
<td>33.6</td>
<td>36.4</td>
<td>34.4</td>
<td>37.6</td>
</tr>
</tbody>
</table>
appear. For example, the output at the data rate of 21 Gb/s is shown in Fig. 6.28(b). The maximum transmission capacity of the stripline interconnect is concluded to be 13 Gb/s.

From this study, the SIW is shown to provide a wideband transmission medium. It is further demonstrated that such a channel can handle maximum data rate of 21 Gb/s when the bandwidth of its system components are sufficiently wide. Therefore, when the hybrid structure of Fig. 6.22 is used in data transmission system with ideal driver and receiver electronics, an aggregate data rate of 47 Gb/s can be achieved.

6.7 Summary

Due to the relatively larger footprint of a waveguide interconnect, a hybrid substrate integrated waveguide is proposed as a method to efficiently utilize the physical channel. The hybrid approach is achieved by routing striplines in and out of the waveguide substrate. In this manner, multiple channel data transmission is achieved in a compact and enclosed structure with minimal crosstalk due to the use of different modes. The coupling between the two different channels, *i.e.*, TEM and TE_{10} modes, has shown to be negligible. Transition structures needed for embedding striplines inside the waveguide are also proposed. The side-entry transition appears to be a better choice due to maintaining excellent iso-
Fig. 6.28 Simulated data transmission through the stripline portion of the hybrid SIW prototype. Output eye diagrams for data rates: (a) 13 Gb/s. (b) 21 Gb/s.

Simulation between the propagating modes. Hybrid prototypes with single and two embedded striplines are designed, fabricated and evaluated through S-parameter and high-speed system measurements. The hybrid structures demonstrated to be viable for multiple channel high-speed baseband signaling. In the case of two embedded striplines, which provides maximum aggregate data rate of 15 Gb/s, excellent output eye quality was observed. Furthermore, a comparative study using system simulations is presented to demonstrate the ultra-high-speed transmission capacity of 21 Gb/s using the waveguide channel.
Chapter 7

Multimode Substrate Integrated Waveguide

7.1 Introduction

In Chapter 6, a hybrid approach was proposed to increase channel capacity by adding more physical links within the same substrate volume. A conceptual multiport presentation of this hybrid structure is shown in Fig. 7.1(a). Alternatively, the waveguide volume can be utilized as a multimode conduit for multiple-channel transmission without adding new physical interconnects. Similar to the hybrid structure, a multiport illustration of the multimode interconnect is shown in Fig. 7.1(b). Multimode waveguides have been traditionally utilized in the antenna feed networks of satellite communication systems. For example, an orthomode transducer is employed in these systems to distinguish between the orthogonal modes used for transmitting and receiving signals through the same waveguide medium [111, 112]. With the growing interest in application of substrate integrated waveguides in electronic systems, exploiting the multimode capacity of the SIWs and introduction of multimode SIW components are expected. In fact in [113], a multimode SIW was used as an antenna feed to produce sum or difference beams. In this chapter, a substrate integrated waveguide is utilized as a multimode transmission medium. In this manner, no physical channels are required for guiding the orthogonal modes that bear no coupling in propagation within the same transmission medium. Efficient multimode launchers are developed herein, and a multimode data transmission system is implemented to demonstrate
7.2 Multimode Transmission in a Substrate Integrated Waveguide

In Section 7.2, the bandwidth and performance of the hybrid and multimode structures are compared. An efficient transition for exciting the TE\(_{20}\) mode is introduced in Section 7.3. The performance of the multimode double launcher is investigated in Section 7.4. In Section 7.5, a few fabricated prototypes are experimentally characterized to validate the multimode concept. In addition, time-domain measurements are used to confirm the transmission quality of the proposed design for a data rate of 1 Gb/s/channel.

![Multimode Transmission in a Substrate Integrated Waveguide](image)

**Fig. 7.1** Illustration of multimode transmission in a substrate integrated waveguide (SIW). (a) Hybrid SIW. (b) Multimode SIW.

7.2 Multimode Transmission in a Substrate Integrated Waveguide

Conventional solid rectangular waveguides can support transverse electric (TE) and transverse magnetic (TM) modes. However, in an SIW, only TE\(_{m0}\) modes are supported as shown in [106]. TM longitudinal currents on the sidewalls are not supported when the via sidewalls are not connected. TE\(_{m0}\) modes are orthogonal; therefore, a number of them can be used for sending various signal channels with minimum crosstalk through a waveguide. In this work, the parallel signaling system is created without adding a physical interconnect, and the first two TE modes of the waveguide are used for multichannel transmission. Similar to the hybrid structure, a multiport illustration of the studied multimode waveguide is shown in Fig. 7.1(b). Even though possible, increasing the number of signalling channels using higher order modes have been avoided herein due to practical difficulties in

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dual-channel parallel transmission through the substrate integrated waveguide.
exciting several modes simultaneously. This will become obvious when the implementation aspects of the multimode waveguide are discussed.

To compare the operation bandwidths of the two hybrid and multimode SIW structures, individual signaling channels, \(i.e.,\) the \(\text{TE}_{10}\) and \(\text{TE}_{20}\) waveguide modes and the transverse electromagnetic (TEM) mode of the embedded stripline, are investigated. The waveguide and hybrid waveguide structures are simulated using a low-loss substrate (Rogers RO4350B with \(\epsilon_r = 3.48\) and \(\tan\delta = 0.0037\) measured at 10 GHz). The substrate thickness of the waveguide is 0.915 mm. The width of the waveguide, \(W_g = 5.8\) mm, is designed to exhibit the \(\text{TE}_{10}\) cutoff frequency of 14 GHz. The stripline channel is assumed to have the same dielectric thickness as the waveguide, and its width (0.5 mm) is chosen to yield a characteristic impedance of 50 Ω. A finite element method (FEM) solver, Ansoft HFSS [25], is used to derive the transmission characteristics of the waveguide and stripline.

Fig. 7.2 shows the transmission coefficients (labeled as “Stripline” and “\(\text{TE}_{10}\)” ) of a 200-mm long hybrid structure. For the case of multimode waveguide, the same length is considered and the transmission coefficients of its considered propagating modes, \(\text{TE}_{10}\) and \(\text{TE}_{20}\), are shown in the same figure. It can be observed that the transmission coefficient of stripline rolls off with a slightly sharper slope compared to those of waveguide modes. This results in different 3-dB bandwidth measured with respect to the respective maximum transmission coefficient. The 3-dB bandwidths of all the modes are summarized in Table 7.1. If no dispersion compensation technique is included, the operation bandwidth of the waveguide modes are less than the numbers shown in Table 7.1. Nonetheless, it should be pointed out that the dispersive region of the waveguide is close to its cutoff frequency \((f_c)\) and reaches up to \(1.86f_c \) [114]. This reduces the operation bandwidth of \(\text{TE}_{10}\) and \(\text{TE}_{20}\) to 18.3 and 15.4 GHz (beyond 60 GHz is not shown in Fig. 7.2), respectively, which is still larger than that of the stripline.

\[104\]

<table>
<thead>
<tr>
<th>Interconnect/Mode</th>
<th>3-dB Bandwidth (GHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Stripline/TEM</td>
<td>10.3</td>
</tr>
<tr>
<td>Waveguide/(\text{TE}_{10})</td>
<td>32.3</td>
</tr>
<tr>
<td>Waveguide/(\text{TE}_{20})</td>
<td>&gt; 29.5</td>
</tr>
</tbody>
</table>
7.3 Excitation of the TE$_{20}$ Mode

In order to excite the TE$_{20}$ mode, the field profile shown in Fig. 7.3 should be generated. Two coplanar microstrip-to-waveguide transitions are used to generate two out-of-phase field vectors at the waveguide input, as illustrated in Fig. 7.4. This technique is similar to the work described in [113]. An alternative method is to place one of the coplanar transitions on the opposite planes when both transition sections are carrying in-phase signals. This technique is implemented in the structure discussed in Section 7.5.3.

Fig. 7.3 Electric field distribution of TE$_{20}$ mode in a rectangular waveguide.

To investigate the type of transition shown in Fig. 7.4, Ansoft HFSS is used in the simulations. Rogers RO4350B is considered as the substrate material with the substrate thickness of 0.508 mm. The waveguide has the following dimensions: $W_g = 8.6$ mm, $a = 1$ mm, and $D = 0.508$ mm. The total length of the waveguide section is 15 mm. The cutoff frequency of the TE$_{20}$ mode is approximately 18.2 GHz. $W_{m2}$ is chosen to be 1.1 mm in order to obtain a characteristic impedance of 50 $\Omega$.

In the simulation setup, port 1 is excited by differential and common modes (denoted...
by DM and CM) whereas port 2 monitors the incoming waveguide modes (TE_{10}, TE_{20}, and TE_{30}). To excite the TE_{20} mode efficiently, the center of each coplanar transition should be at the locations where the maximum magnitude of the electric field is expected to occur, \( D_t = W_g/2 \). This is confirmed by parametric fullwave simulations, the results of which are not shown here for brevity. Another set of parametric studies is performed to optimize the layout of the transition section. \( W_{m2} \) and \( L_{t2} \) are found to be 1.8 mm and 2.4 mm, respectively, for the best transmission performance. These final dimensions are used in the field solver to calculate the S-parameters of the structure, as presented in Fig. 7.5. In Fig. 7.5(a), the reflection, S(1:DM,1:DM), and transmission, S(2:TE_{20},1:DM), coefficients are presented when port 1 is excited by a differential mode. Note that port 1 is the combined port of the two microstrip lines. It can be observed that TE_{20} waves are efficiently excited in the waveguide and received at port 2 at the frequencies above the cutoff (better than 0.9 dB of insertion loss except around the cutoff). However, if port 1 is excited by a common mode, this is not the case as shown in Fig. 7.5(b) by S(2:TE_{20},1:CM) plot. Overall, it can be seen that the coupling of energy from common mode to TE_{20} mode is insignificant (below -30 dB up to 40 GHz). In the same figure, the coupling from differential mode excitation to TE_{10} mode are also presented, which is less than -29 dB across the studied frequency range. This type of parameter should be inspected in designing launchers for multimode excitation.

Fig. 7.4 A coplanar microstrip TE_{20} transition.
Finally, to confirm excitation of the TE$_{20}$ mode using the proposed transition with differential excitation, the electric field distribution along the waveguide is plotted as shown in Fig. 7.6 at 40 GHz.

![Simulated S-parameters of an SIW with coplanar microstrip TE$_{20}$ transitions. (a) Reflection and transmission coefficients. (b) Mode coupling coefficients.](image1)

![Magnitude of the electric field distribution of the TE$_{20}$ mode at 40 GHz.](image2)
To use the structure of Fig. 7.4 for multimode signaling, TE_{10} mode should be excited as well. For this purpose, a multimode double launcher is suggested in Fig. 7.7. The fundamental TE_{10} is excited by employing a via transition [66]. To ensure propagation of the excited TE_{10} mode in the desired direction, a fin line is inserted in the waveguide as shown in the figure. The fin line essentially creates two waveguide sections with half of the original width, i.e., W_g/2, therefore, yielding twice the cutoff frequency of the original TE_{10} mode for their dominant mode cutoff. As a result, this wall will block the backward propagation of the TE_{10} mode excited by the via transition.

![Fig. 7.7](image_url)  
**Fig. 7.7** A multimode double launcher for simultaneous excitation of TE_{10} and TE_{20} in an SIW.

To study the performance of the proposed multimode double launcher, Ansoft HFSS is used to analyze the structure of Fig. 7.7. To reduce the computational size and expedite simulations, the via walls are replaced by solid conductor walls. Our simulations proved that implication of this simplification on the accuracy of the results is very negligible. The waveguide (W_g = 8.6 mm) and coplanar TE_{20} mode launcher have the same dimensions as those described in Section 7.3. The TE_{10} and TE_{20} cutoff frequencies of the waveguide are 9.35 GHz and 18.7 GHz, respectively. A microstrip line (W_{m1} = 1.1 mm) connecting the via post (D_h = 0.508 mm) to port 3 is routed at 0.508 mm above the waveguide section.
From parametric fullwave simulations, the parameters related to the via transition and fin line are found to be $D_{\text{edge}} = 1 \text{ mm}$, $D_{\text{vf}} = 2.5 \text{ mm}$, $D_{\text{vg}} = 0.908 \text{ mm}$, and $L_f = 6.5 \text{ mm}$. The total length of the waveguide section is 25 mm.

The transmission performance of the structure under study is monitored as shown in Fig. 7.8(a). Specifically, $S(2:\text{TE}_{20},1:\text{DM})$, represents the transmission quality of the TE$_{20}$ channel as it is an indicator of the TE$_{20}$ energy detected at port 2 when port 1 is excited by the differential mode. The minimum insertion loss is found to be -1 dB and its 3-dB bandwidth extends from 19.1–40 GHz and beyond. For the TE$_{10}$ channel, $S(2:\text{TE}_{10},3:\text{Q-TEM})$ shows the level of the TE$_{10}$ signal received when the microstrip at port 3 is excited by the quasi-TEM mode. The minimum insertion loss of this channel is -0.62 dB having the 3-dB bandwidth between 9.7–18.5 GHz. The sharp drop in the transmission of the TE$_{10}$ channel around and beyond 20 GHz is attributed to the coupling of the signal into port 1. It should be pointed out that the fin-line section acts as a power divider, which allows the TE$_{10}$ mode to pass through when the frequency exceeds the TE$_{10}$ cutoff frequency of this power divider section (18.7 GHz). As a result, these waves are coupled into the coplanar strips of port 1 mostly in the form of a common mode. This observation is confirmed by the $S(1:\text{CM},3:\text{Q-TEM})$ parameter, which keeps rising as frequency increases above 18.7 GHz, as shown in Fig. 7.8(b). On the contrary, the coupling to the differential mode, i.e., $S(1:\text{DM},3:\text{Q-TEM})$, is quite insignificant—generally well below -28.5 dB (not shown here for brevity). Another important parameter is coupling from the TE$_{10}$ mode to the TE$_{20}$ mode along the multimode waveguide section, which is measured by $S(2:\text{TE}_{20},3:\text{Q-TEM})$ as presented in Fig. 7.8(b). The magnitude of this coupling indicator is found to be negligible within the useful bandwidth of the TE$_{10}$ channel as marked in Fig. 7.8(a). However, it rises above -40 dB from 18.5 GHz and maintains below -23 dB over the studied frequency band. Overall, the bandwidth of the TE$_{20}$ channel is observed to be relatively wide whereas the TE$_{10}$ channel bandwidth is limited by the effectiveness of the fin line. In order to avoid the consequence of the $S(1:\text{CM},3:\text{Q-TEM})$ coupling, the bandwidth of the signal entering port 3 (TE$_{10}$ channel) should not cover beyond the cutoff frequency of the TE$_{20}$ mode. Additionally, the circuits preceding port 1 should have high common-mode rejection to ensure minimum crosstalk in the multimode channels.

As discussed in the previous study, the bandwidth provided by the TE$_{10}$ channel is significantly lower than that of the TE$_{20}$ channel. It is possible to increase the TE$_{10}$ channel bandwidth by reducing the waveguide width at the entry point connecting the coplanar
TE_{20} transition at port 1, as shown in Fig. 7.9. Fullwave simulations are performed on this modified structure for \( W_{g2} = 6.2 \) mm. Effectively, the TE_{20} cutoff frequency is raised from 18.7 GHz to 25.9 GHz. As shown in Fig. 7.10, the TE_{10} channel 3-dB bandwidth of the new structure is extended to be between 9.9–23.3 GHz. It can be observed that this method comes at the cost of increasing the cutoff frequency the TE_{20} mode; for instance in this case, it is shifted from 19.1 GHz to 26.6 GHz. Mode coupling analysis of this structure, which is not shown here for brevity, also presents similar characteristics as those described in Fig. 7.8(b).

7.5 Experimental Evaluations

In order to validate the multimode concept experimentally, several structures were prototyped in Rogers 4350B substrates using a multilayer PCB fabrication process. Since a multimode SIW is a 4-port device, the structure has been designed and characterized up to the maximum frequency of 20 GHz. This was dictated by the measurement frequency range of the available multiport vector network analyzer.
7.5 Experimental Evaluations

Fig. 7.9 A multimode double launcher with tapered waveguide to increase the TE\textsubscript{10} channel capacity.

7.5.1 Coplanar Microstrip TE\textsubscript{20} Transition Prototype

First, the coplanar microstrip TE\textsubscript{20} transition discussed in Section 7.3 is validated by using frequency-domain measurements. The fabricated prototype, as shown in Fig. 7.11, consists of two coplanar transitions at both ends. The waveguide section has been designed to exhibit the TE\textsubscript{20} cutoff frequency of 11.3 GHz. Therefore, the waveguide dimensions according to Fig. 7.4 are chosen to be $W_g = 14$ mm, $a = 1$ mm, and $D = 0.508$ mm. The overall thickness of the Rogers RO4350B substrate is 1.016 mm, and $W_{m2}$ is found to be 2.1 mm for a 50-Ω microstrip line. Determined from parametric fullwave simulations, the optimum values of $W_{t2}$ and $L_{t2}$ are 3.2 mm and 3 mm, respectively. All other dimensions are included in Fig. 7.11. SubMiniature version A (SMA) connectors are attached to the microstrip ports for measurements with a coaxial system.

An Anritsu 37397D vector network analyzer in conjunction with an SM5962 multiport test set are used to perform single-ended 4-port measurements. These 4-port S-parameters are subsequently converted to mixed-mode S-parameters [115]. Fig. 7.12 shows the measured mixed-mode S-parameters of the prototype understudy. In addition, fullwave simulated results are also included for comparison. It should be noted that the combined single-ended ports in Fig. 7.11 are labeled as ports 1 and 2. The propagation charac-
Fig. 7.10 Transmission performance evaluation of the multimode double launcher with tapered sections.

![Multimode Substrate Integrated Waveguide](image)

Fig. 7.11 A fabricated coplanar microstrip TE\textsubscript{20} transition prototype.

teristics of the TE\textsubscript{20} in an SIW is represented by \( S_{dd}\)-parameters or \( S(1:DM,1:DM) \) and \( S(2:DM,1:DM) \), \textit{i.e.}, reflection and transmission coefficients, respectively, as shown in Fig. 7.12(a). It is observed that the measured cutoff frequency is approximately 11.11 GHz, which is very close to the simulated result of 11.28 GHz (or the design value of 11.3 GHz). The simulated \( S(2:DM,1:DM) \), which also includes the connector models, shows a good TE\textsubscript{20} transmission performance. However, there is a large deviation in the measurements beyond 14 GHz. Similar observation is noted when measuring the conversion between the common and differential modes, as depicted in Fig. 7.12(b). The discrepancies can be attributed to the multiport test set, which does not provide a truly balanced measurement. In order to efficiently excite the TE\textsubscript{20} mode, the two inputs of the coplanar transition must be exactly 180° out of phase. Any deviations will compromise the transmission performance of this mode. It will be shown later that the measurements improve after baluns are incorporated.
7.5 Experimental Evaluations

Fig. 7.12 Measured and simulated mixed-mode S-parameters of the coplanar microstrip TE\textsubscript{20} transition prototype. (a) Reflection and transmission. (b) Mode coupling.

The above argument is supported by examining the common-mode S-parameters, S(1:CM,1:CM) and S(2:CM,1:CM), as shown in Fig. 7.13. When the two inputs of the TE\textsubscript{20} coplanar transition are in-phase, they contribute to create a TE\textsubscript{10} propagating mode inside the waveguide. Therefore, measured and simulated S(2:CM,1:CM) both exhibit a cutoff frequency of approximately 5.4 GHz in Fig. 7.13. A significant drop in S(2:CM,1:CM) transmission coefficient is observed around 16.5 GHz, which is due to the excitation of TE\textsubscript{30} mode.

Fig. 7.13 Measured and simulated common-mode S-parameters of the coplanar microstrip TE\textsubscript{20} transition prototype.
7.5.2 Multimode Double Launcher Prototype

The multimode double launcher introduced in Section 7.4 is investigated experimentally in this section. The fabricated prototype is shown in Fig. 7.14. The base waveguide is the same as the one described in Section 7.5.1. To excite or receive the TE\textsubscript{10} mode, the inner conductor pin of an SMA connector is used and soldered to the bottom conductor plane of the SIW. Fin lines are positioned inside the SIW with $D_{\text{edge}} = 1.254$ mm, $D_{vf} = 3$ mm, and $L_f = 7$ mm at both ends—refer to Fig. 7.7 for the definition of $D_{\text{edge}}$, $D_{vf}$, and $L_f$ parameters.

![Fig. 7.14 A fabricated multimode substrate integrated waveguide.](image)

The TE\textsubscript{20} coplanar transitions are first characterized while ports 3 and 4 are terminated to 50-Ω loads. Fig. 7.15(a) presents the measured $S_{dd}$-parameters, which show a better agreement with the simulated results than those observed in Fig. 7.12(a). This is attributed to the presence of the fin lines which enforce nulls at the mid-width of the SIW and provide a better alignment in launching the differential signals into the waveguide. In addition, as shown in Fig. 7.15(b), the differential-common mode coupling is improved between the TE\textsubscript{10} and TE\textsubscript{20} cutoff frequencies. The fin-line section reduces the possibility of recombination of the differential signals into the TE\textsubscript{10} wave, which is detected as a common-mode output. As a result, the cutoff frequency of S(2:CM,1:CM) is the same as that of the TE\textsubscript{20} mode (see Fig. 7.16). Better correlation between the simulations and measurements is also observed for the common-mode S-parameters.

Additionally, the performance of the TE\textsubscript{10} channel is depicted in Fig. 7.17. In this measurement, each of the microstrip terminals in ports 1 and 2 are connected to 50-Ω terminations. A good agreement between simulations and measurements is observed in this case. The TE\textsubscript{10} cutoff frequency is measured to be 5.45 GHz. Its behavior is very similar to the case discussed in Fig. 7.8(a). For instance, the first dip (13.3 GHz) in the
transmission curve of the TE\textsubscript{10} signal occurs not far from the cutoff frequency of the TE\textsubscript{20} mode. Furthermore, as expected, the fin line is effective in blocking the TE\textsubscript{10} coupling to the TE\textsubscript{20} coplanar ports up to around the cutoff frequency of the TE\textsubscript{20} mode. This is confirmed when the common mode is detected at port 1 while the TE\textsubscript{10} mode is launched from port 3, \textit{i.e.}, S(1:CM,3), as presented in Fig. 7.18. Each SMA connector at port 2 is terminated to 50-\(\Omega\) load. In the same figure, it is observed from simulations that the coupling to the differential mode or S(1:DM,3) is significantly small. However, the measurements indicate a higher level of coupling due to nonideal balanced excitation as discussed earlier. A similar observation has also been noted for the couplings between ports 1 and 4, which are not shown here for brevity.

### 7.5.3 Multimode Double Launcher Prototype with Baluns

To efficiently harness the TE\textsubscript{20} mode for signal transmission, balanced feed launchers are required as indicated in the previous sections. Balun structures are designed and incorporated into the multimode waveguide under study, as shown in Fig. 7.19. A stripline is used to feed single-ended signals into the top and bottom waveguides (operating in a single-mode region), which share the middle conductor plane. The outputs of the waveguide are routed from the top and bottom conductor planes into microstrip lines whose ground reference is
Fig. 7.16 Measured and simulated common-mode S-parameters of the multimode double launcher prototype.

an extension of the middle conductor plane of the single-mode waveguide section. The routing of both microstrip outputs is symmetric, and the signals are considered to be in-phase with respect to the reference ground. In order to provide an out-of-phase excitation into the multimode section, which is equivalent to generating the TE$_{20}$ mode, the microstrip lines are connected to the opposing conductor planes of the multimode waveguide. Hence, balanced signals can be launched into the waveguide.

To incorporate the balun sections into the multimode prototype, fullwave parametric study with Ansoft HFSS is used to design and optimize their dimensions. The width of the 50-Ω stripline is 0.57 mm for the top and bottom conductor spacing of 1.016 mm. The other parameters are found to be $W_{t1} = 2.2$ mm, $L_{t1} = 4$ mm, $W_{g3} = 7.8$ mm, $L_{g3} = 7$ mm, and $W_{mt} = 2$ mm. The fabricated structure is shown in Fig. 7.20. In order to attach SMA connectors to ports 1 or 2 for testing, a microstrip section is added, which is connected to the stripline by a metallized via hole. The multimode section is the same as the one described in Section 7.5.2.

Fig. 7.21(a) shows the reflection and transmission characteristics of the TE$_{10}$ mode, i.e., between ports 3 and 4 of the studied prototype. It can be observed that the performance is quite comparable to that of the multimode structure in Fig. 7.17, especially in the single-mode region. However, the addition of the baluns seems to create sharp dips around 11.8 GHz and 14.5 GHz. The transmission coefficient of the TE$_{20}$ mode between ports 1 and 2 is also presented in Fig. 7.21(b). In general, the performance characteristic of this TE$_{20}$ channel is very similar to that of Fig. 7.15(a) in the frequency range of 11.1–
7.5 Experimental Evaluations

17.2 GHz. It is also observed that the balanced feed launcher is not efficient beyond that frequency band. The coupling coefficients between the TE$_{10}$ and TE$_{20}$ modes, which are measured between ports 1–3 and 1–4, are shown in Fig. 7.22. Excellent correlation between the measured and simulated data is observed in all cases. It can be concluded that the proposed balun structure provides a well-balanced excitation of the differential mode and extends its operation bandwidth.

7.5.4 Multichannel Signal Transmission

To demonstrate dual-channel signaling in the proposed multimode scheme, the fabricated prototype containing baluns as described earlier in Section 7.5.3 is incorporated in a sample parallel bandpass data transmission system. The system setup is shown in Fig. 7.23. In this bandpass transmission system, which is similar to the one introduced in [116], mixer are used to upconvert a baseband signal to the desired carrier frequency. The baseband signals are stream of pulses generated by a pseudo-random binary sequence pulse pattern generator. These upconverted signals are sent through the TE$_{10}$ and TE$_{20}$ channels simultaneously, and they are recovered by a pair of receiver mixer and lowpass filter. A 1-Gb/s pseudo-random binary sequence with peak-to-peak amplitude of 250 mV is supplied by each output of the pulse pattern generator. As shown in Fig. 7.24, output eye diagrams of the TE$_{10}$ and TE$_{20}$ channels are monitored by a dual-channel 80E02 (12-GHz bandwidth) electrical sampling module on a Tektronix TDS8200 oscilloscope. It can be seen that the output eye heights
Fig. 7.18 Measured and simulated coupling between the TE_{10} and TE_{20} modes in the multimode double launcher prototype.

are reduced, which is caused by the conversion loss of the mixers. Overall, excellent output eye quality is observed at the data rate of 1 Gb/s in this multimode parallel transmission system. In order to achieve higher data rates, wider bandwidth transitions and mode launchers should be used.

This experiment demonstrates the use of multimode substrate integrated waveguides in parallel signal transmission. Like any parallel system, it adds to the electronics overhead and increases the number of drivers and receivers. However, it does not require an additional physical link because of mode orthogonality. In addition to the presented bandpass data transmission system, the potential applications of this approach include multichannel RF signal routing at the front end of telecommunication systems.

7.6 Summary

In this chapter, a multimode concept is proposed to achieve multi-channel data transmission in substrate integrated waveguides. The orthogonal TE_{10} and TE_{20} modes are employed to demonstrate the concept. An efficient coplanar microstrip TE_{20} transition for exciting TE_{20} modes is also introduced, which is shown to be low-loss and wideband. In addition, a multimode double launcher is proposed in order to provide simultaneous transmission of the TE_{10} and TE_{20} channels along the shared waveguide medium. The via transition is utilized to launch the TE_{10} mode in the double launcher structure. In order to minimize coupling between the two channels, a fin line is included in the multimode double launcher. As a
Fig. 7.19 A balun for exciting the TE\(_{20}\) mode in an SIW.

result, the bandwidth of the TE\(_{10}\) channel, which is limited between the cutoff frequency of the TE\(_{10}\) and TE\(_{20}\) modes, is significantly less than that of the TE\(_{20}\) channel. By reducing the waveguide width near the input of the coplanar TE\(_{20}\) transition, the TE\(_{10}\) channel bandwidth can be improved significantly. Several prototypes were fabricated to validate the concept experimentally. A truly balanced structure is required to efficiently generate the needed differential-mode input at the coplanar microstrip TE\(_{20}\) transition. An SIW-based balun is proposed herein for this purpose. Both simulations and measurements are used to verify the effectiveness of the baluns. It is demonstrated that excellent eye qualities are obtained when 1-Gb/s data are transmitted through both the TE\(_{10}\) and TE\(_{20}\) channels simultaneously. Overall, the proposed technique is proved to be an effective method of creating two communication channels in the same substrate integrated waveguide.
Fig. 7.20 A fabricated multimode SIW with baluns.

Fig. 7.21 Measured and simulated S-parameters of the multimode double launcher prototype with baluns. (a) TE$_{10}$ mode. (b) TE$_{20}$ mode.

Fig. 7.22 Measured and simulated coupling parameters of the multimode double launcher prototype with baluns.
Fig. 7.23 Measurement setup of a multimode SIW for dual-channel data transmission.

Fig. 7.24 Output eye diagrams of a dual-channel multimode SIW at a data rate of 1 Gb/s.
Chapter 8

Conclusions

8.1 Thesis Summary

In this thesis, a bandpass waveguide-based interconnect was proposed as an alternative means for ultra-high-speed data transmission. The substrate integrated waveguide (SIW) is essentially a rectangular waveguide formed in a circuit substrate. It can be fabricated using common printed circuit board (PCB) fabrication technologies. SIW provides low-loss, wide-band signal transmission in a shielded structure. With inclusion of proper driver and receiver stages, it enables ultra-high-speed data transmission, thus offering an all-electrical-domain signaling solution, which is more attractive compared to optical interconnects in short-range communications due to low cost and ease of integration.

In this thesis, a systematic approach based on electromagnetic bandgap concept was employed to the design of the waveguide interconnect. This ensures negligible leakage from the sidewalls. From fullwave simulations, the waveguide was characterized and found to exhibit the smallest insertion loss in comparison with traditional planar interconnects, especially for the case of thin substrates used in modern multilayer PCBs and packages. Furthermore, three different waveguide bends were suggested and demonstrated to be very efficient in guiding signals around sharp corners. Further signal integrity analysis showed that the isolation between two waveguide interconnects with a common sidewall is excellent rendering low crosstalk interconnects. SIW needs transition sections to adapt to planar circuits. The coplanar microstrip-to-waveguide transition tend to create a weak point decreasing isolation between the two waveguides. Hence, via fence structures were proposed and incorporated in the transition sections to improvement crosstalk immunity.
Two main integration challenges for including SIW interconnects in high-speed baseband systems were identified and addressed in this thesis. Firstly, the via and aperture transitions were investigated for 3-D integration of waveguide interconnects. Their respective lumped equivalent circuit models were proposed to enable spice-like simulations and faster turn-around time in design and optimization. As well, error analysis was performed by using fullwave parametric studies in order to determine the validity range of the developed models with layout and frequency variations. The via and aperture transition models were shown to be valid between 10.35–19.10 GHz and 10.1–28 GHz, respectively, considering a maximum error of 15%. Measurements of the fabricated prototypes containing the studied transitions also showed good correlation with the proposed models. To address the second challenge due to the bandpass characteristic of the waveguide interconnects, driver and receiver blocks that accommodate high-speed baseband transmission were introduced. Mixers are used for the up-conversion and down-conversion of the baseband signals. A lowpass filter is also incorporated in the receiver section to recover baseband signals. The proposed waveguide interconnect system was experimentally evaluated and demonstrated to handle high-speed data rates of up to 5 Gb/s with excellent output eye qualities. The incurred transmission loss were mainly due to the conversion loss of the off-the-shelf mixers used in the system. The fabricated SIW prototype was measured to be very wideband (3-dB bandwidth of 19 GHz). However, the bandwidth of the system components was the limiting factor in achieving higher transmission rates. In fact, in one particular experiment which was not shown in the thesis for brevity, it was found that when system components with wider bandwidth were used transmission rate of 10 Gb/s was achieved.

The size of the substrate integrated waveguides is a concern in utilizing them in a compact routing environment. To alleviate this shortcoming, two approaches based on reusing the waveguide channel were proposed in this thesis. In the first method, a hybrid substrate integrated waveguide creates multiple transmission channels by embedding stripline interconnects inside the waveguide. The side-entry transition was shown to be an efficient way of routing striplines in and out of the waveguide. The characteristic impedance of the stripline is unaffected as long as the interconnect is placed sufficiently far from the sidewalls. Mode coupling analysis showed negligible interactions between the waveguide and stripline channels. Aggregate transmission rate of 15 Gb/s with excellent output eye qualities was achieved using a hybrid SIW system with two embedded striplines. Finally, in the second technique, a multimode SIW reuses the physical waveguide channel by em-
ploying two orthogonal TE$_{10}$ and TE$_{20}$ modes for signal transmission. A low-loss wideband coplanar transition was proposed to launch and receive the TE$_{20}$ mode. Subsequently, a multimode double launcher was designed to provide simultaneous excitation of both the TE$_{10}$ and TE$_{20}$ modes. This double launcher showed a reduced bandwidth for the TE$_{10}$ channel and a relatively higher coupling between the TE$_{10}$ and TE$_{20}$ channels due to its structural characteristics. Overall, the hybrid SIW was shown to provide wider bandwidth compared to multimode SIW.

8.2 Future Work Recommendations

The work in this thesis demonstrates the feasibility of using bandpass waveguide interconnects for high-speed signal transmission. As the research is still in the early stage, there are several directions of research can be undertaken to improve cost and performance. These recommendations are outlined below.

1. In the implementation of waveguide-based interconnect system, off-the-shelf mixers were used for modulation and demodulation of the baseband signals. High conversion loss of the driver and receiver mixers significantly reduce the system output amplitude. The mixer's IF bandwidth is also another factor limiting the maximum achievable data rate. Therefore, mixer design, which should be optimized for this high-speed bandpass channel, is viewed as an important step to make this approach transferable to industry and competitive with other baseband signaling techniques. The mixer specifications should be aimed for high frequency, wide bandwidth and low power operation while being low cost. These can be achieved in CMOS technology.

2. The modulation technique employed in this work is a basic type and based on binary phase shift keying. Although it provides higher SNR compared to other methods, the channel bandwidth usage is not very efficient due to the double sideband modulation. To further increase the channel capacity, QPSK and QAM, for instance, can be employed. Multi-level signaling techniques described in Chapter 2 are other viable alternatives. All of these methods come at the cost of increased complexity and power consumption, and thorough investigations must assess their feasibilities.

3. The waveguide interconnect is a dispersive channel, which can cause distortion in the output waveforms. Therefore, dispersion compensation is another important research
area that should be followed in order to further improve the system bandwidth and performance. For instance, digital filters, which are widely used in equalization, could provide a potential solution.

4. The multimode transmission concept was demonstrated in Chapter 7 to reutilize the waveguide substrate, and, at the same time, increase its channel capacity. The performance of the proposed multimode double launcher, however, limits the bandwidth of the individual channels. To enable a broadband multimode solution, alternative structures for multimode excitation must be investigated. In addition, the hybrid approach could be integrated with the multimode structure to further increase aggregate channel capacity, and, therefore, the signal integrity impact must be examined.
Appendix A

Brillouin Zone of a Square Lattice

In order to describe the behavior of the electromagnetic (EM) wave propagation in a medium, a dispersion relation is often used. Specifically, it provides a relationship between the wave vector (or phase progression) and frequency. For a particular polarization of an incident wave, higher order modes besides the fundamental one may exist inside the medium. For instance, TE$_{20}$ mode can propagate through a rectangular waveguide when operating beyond its cutoff frequency. Detailed explanation of dispersion relation can be found in [38].

The electromagnetic bandgap (EBG) structure presented in Chapter 3, Fig. 3.2, has essentially a non-homogeneous substrate. Due to the 2-D periodic nature of the EBG structure, it would be redundant to compute eigenvalues for every possible direction. Hence, the Brillouin zone (to be more specific the irreducible Brillouin zone) is used to characterize the dispersion response for non-redundant wave vectors [8]. Once these unique wave vectors are found, propagation directions lying outside the Brillouin zone can be calculated by using the translational symmetry of the reciprocal lattice vectors of the structure.

The lattice constant or periodicity is often described by the width of the unit cell along the considered direction of the periodic structure. In the case studied in Chapter 3, the EBG substrate has a square lattice whose lattice constant is $a$. In a square lattice as depicted in Fig. A.1, the lattice vectors can be defined as $\mathbf{a}_1 = a\hat{x}$ and $\mathbf{a}_2 = a\hat{y}$. Consequently, its reciprocal lattice vectors are found to be $\mathbf{b}_1 = (\frac{2\pi}{a})\hat{x}$ and $\mathbf{b}_2 = (\frac{2\pi}{a})\hat{y}$. According to [8], the first Brillouin zone is constructed as follows. First, the center point of the reciprocal lattice structure is taken as the origin. The (dashed) lines are then used
to connect the center points of adjacent cells. Subsequently, perpendicular bisectors (solid lines) are drawn for every lattice vector that begins at the origin. The Brillouin zone is formed within the intersection of these bisectors; it is the highlighted square in Fig. A.1. The irreducible Brillouin zone of this lattice, which carry the information of non-redundant wave vectors, is configured within highlighted square by the dashed lines. It can be seen that the irreducible Brillouin zone of a square lattice has a triangular shape as shown in Fig. A.1 and in the inset of Fig. 3.4. This is the smallest region within the Brillouin zone for which the wave vectors are not related by symmetry whereas the rest of the Brillouin zone consists of redundant copies of the irreducible zone [8].

Fig. A.1  The square lattice and its first Brillouin zone [8].
Appendix B

Review of Orthogonality in TE$_{mn}$ and TM$_{mn}$ Modes

B.1 TE Modes

In this appendix, it is shown that the TE modes in a rectangular waveguide are orthogonal. First, let the width (along x-axis) and height (along y-axis) of the waveguide be $a$ and $b$, respectively. The direction of propagation is in the z-direction. From [117], the solutions of the TE$_{mn}$ mode for $0 \leq x \leq a$ and $0 \leq y \leq b$ are expressed as:

\begin{align*}
E_x &= E_{x,mn}^0 \cos\left(\frac{m\pi x}{a}\right) \sin\left(\frac{n\pi y}{b}\right), \quad (B.1a) \\
E_y &= E_{y,mn}^0 \sin\left(\frac{m\pi x}{a}\right) \cos\left(\frac{n\pi y}{b}\right), \quad (B.1b) \\
H_x &= H_{x,mn}^0 \sin\left(\frac{m\pi x}{a}\right) \cos\left(\frac{n\pi y}{b}\right), \quad (B.1c) \\
H_y &= H_{y,mn}^0 \cos\left(\frac{m\pi x}{a}\right) \sin\left(\frac{n\pi y}{b}\right). \quad (B.1d)
\end{align*}

where $E_{x,mn}^0 = \frac{i\omega \mu n}{k_c b} A_{mn}$, $E_{y,mn}^0 = \frac{-i\omega \mu m}{k_c a} A_{mn}$, $H_{x,mn}^0 = \frac{j\beta n}{k_c b} A_{mn}$, $H_{y,mn}^0 = \frac{j\beta m}{k_c a} A_{mn}$, and $k_c = \sqrt{\left(\frac{m\pi}{a}\right)^2 + \left(\frac{n\pi}{b}\right)^2}$. The propagation term, $e^{-j\beta z}$, is dropped for convenience.

The definition of orthogonality [118] states that functions $y_1, y_2, \ldots$ defined in $c \leq x \leq d$ interval are orthogonal over the same interval with respect to a weight function $p(x) > 0$ if

\[ \int_c^d p(x) y_m(x) y_n(x) dx = 0. \quad (B.2) \]
By the same token, the orthogonality between TE\textsubscript{ij} and TE\textsubscript{uv} modes for \( E_y \) over the intervals \( 0 \leq x \leq a \) and \( 0 \leq y \leq b \) can be found from

\[
\int_0^b \int_0^a E^0_{y,ij} E^0_{y,uv} \sin\left(\frac{i\pi x}{a}\right) \cos\left(\frac{j\pi y}{b}\right) \sin\left(\frac{u\pi x}{a}\right) \cos\left(\frac{v\pi y}{b}\right) dx dy. \tag{B.3}
\]

Dropping the constant terms and re-arranging (B.3) result in

\[
\int_0^b Y(y) \int_0^a X(x) dx dy \tag{B.4}
\]

where

\[
X(x) = \sin\left(\frac{i\pi x}{a}\right) \sin\left(\frac{u\pi x}{a}\right) \tag{B.5a}
\]

\[
Y(y) = \cos\left(\frac{j\pi y}{b}\right) \cos\left(\frac{v\pi y}{b}\right). \tag{B.5b}
\]

By using the trigonometric identities, equation (B.5a) is simplified as follows:

\[
X(x) = \frac{1}{2} \cos\left(\frac{i - u}{a} \pi x\right) - \frac{1}{2} \cos\left(\frac{i + u}{a} \pi x\right) \tag{B.6}
\]

Subsequently, the inner integral of (B.4) is found to be

\[
\int_0^a X(x) dx = \left[ \frac{a}{2\pi(i - u)} \sin\left(\frac{i - u}{a} \pi x\right) - \frac{a}{2\pi(i + u)} \sin\left(\frac{i + u}{a} \pi x\right) \right]_0^a \tag{B.7}
\]

Hence, \( \int_0^a X(x) dx = 0 \) for all \( i, u \in \mathbb{Z}^+ \). It is also noted that \( i \neq u \). The same argument is also applied to \( \int_0^b Y(y) dy = 0 \) for all \( j, v \in \mathbb{Z}^+ \) and \( j \neq v \).

Similarly, it can be shown that \( E_x, H_x \) and \( H_y \) components are orthogonal when \( i \neq u \) and \( j \neq v \). Therefore, TE\textsubscript{ij} and TE\textsubscript{uv} modes are orthogonal.
B.2 TM Modes

The solutions of the TM$_{mn}$ mode for $0 \leq x \leq a$ and $0 \leq y \leq b$ are expressed as [117]:

\[
\begin{align*}
E_x &= E_{x,mn}^1 \cos\left(\frac{m\pi x}{a}\right)\sin\left(\frac{n\pi y}{b}\right), \\
E_y &= E_{y,mn}^1 \sin\left(\frac{m\pi x}{a}\right)\cos\left(\frac{n\pi y}{b}\right), \\
H_x &= H_{x,mn}^1 \sin\left(\frac{m\pi x}{a}\right)\cos\left(\frac{n\pi y}{b}\right), \\
H_y &= H_{y,mn}^1 \cos\left(\frac{m\pi x}{a}\right)\sin\left(\frac{n\pi y}{b}\right).
\end{align*}
\]

where $E_{x,mn}^1 = -j\frac{\beta_m \pi}{ak_z} B_{mn}$, $E_{y,mn}^1 = -j\frac{\beta_n \pi}{bk_z} B_{mn}$, $H_{x,mn}^1 = j\frac{\omega \epsilon n \pi}{bk_z} B_{mn}$, $H_{y,mn}^1 = -j\frac{\omega \epsilon m \pi}{ak_z} B_{mn}$, and $k_z = \sqrt{\left(\frac{m\pi}{a}\right)^2 + \left(\frac{n\pi}{b}\right)^2}$. The propagation term, $e^{-j\beta z}$, is again dropped for convenience.

It is observed from (B.8) that the electric and magnetic fields have similar sine and cosine relationships as those of the TE mode in (B.1) except for the constant terms. By using similar arguments earlier, it can be shown that the TM modes are also orthogonal.

B.3 TE and TM Modes

Again, due to the similarity between the electric and magnetic fields of the TE and TM modes, the TE and TM modes are therefore orthogonal.
References


References


