Monolithic Nyquist Rate Analog to Digital Converter With Digital Calibration

by
Yang Wu, B. Eng. 1998

Department of Electrical Engineering
McGill University, Montréal

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Abstract

Nyquist rate analog to digital converter have always been an essential component in complex systems ranging from digital oscilloscope, radar, to modern telecommunication equipments. The fast-paced development in these complex systems has necessitated methods to improve resolution and power consumption of the analog to digital converters. The aim of this thesis is to offer one such method. The method involves the application of a digital DC reference source. The digital reference source will be proposed and used to remove mismatch, reduce comparator offset, thus improving the resolution of both flash and pipeline ADCs, while consuming no static power. The design of pipeline ADCs is also the emphasis of this work.

The digital reference source consists of flip-flops and RC low-pass filters. By programming flip-flops with appropriate digital bit streams, accurate DC reference levels can be generated. The generated DC reference levels replace the need for reference ladder in Flash ADCs. Furthermore, with programmability provided by the digital reference source, the generated reference levels can be modified to reduce comparator offset. The comparator offset reduction algorithm is also applied to pipeline ADCs to reduce non-linear distortion.

The design details of pipeline ADC is also discussed in this work. Quantitative analyses have been provided in determining design parameters in various subsystems. The analyses ensure that a 10-bit resolution is achieved for the pipeline ADC. Both Flash ADC and pipeline ADC were implemented in a 0.25 μm and 0.18 μm CMOS process respectively, and results demonstrating their successful operation are presented.
Résumé

Le convertisseur analogique-digital à la cadence de Nyquist ont toujours été un composant essentiel dans les systèmes complexes s'étendant de l'oscilloscope à l'échantillonnage digitale, radar, aux matériels modernes de télécommunication. Le développement rapide dans ces systèmes complexes a rendu nécessaire l'amélioration de la précision et de la consommation d'énergie des convertisseurs analogique-digital.

Le but de cette thèse est de proposer une telle méthode. Cette méthode consiste à introduire l'applications de source de référence digitale. La référence digitale sera utilisée pour corriger l'erreur de géométrie relative, réduire le décalage de comparateur, de ce fait améliorant la précision des convertisseur de type flash et pipeline, sans consommer de puissance statique. La conception de convertisseur analogique-digital (ADC) est également soulignée dans ce travail.

La source digitale de référence est construite à partir de bascules et des filtres RC passe-bas. En programmant des bascules avec les séquences binaires digitaux appropriés, des niveaux de référence précis de C.C peuvent être produits. Les niveaux de référence C.C produits élimine le besoin d'échelle de référence dans les ADCs de type flash. En plus, avec la programmabilité fournie par la source digitale de référence, les niveaux de référence produits peuvent être modifiés pour réduire le décalage de comparateur. L'algorithme de réduction de décalage de comparateur est également appliqué aux ADCs de type pipeline pour réduire la déformation non linéaire introduite par le décalage du comparateur.

Les détails sur la conception de ADC de type pipeline sont également présentes dans ce travail. Des analyses quantitatives ont été fournies pour déterminer des paramètres de conception dans divers sous-systèmes. Les analyses s'assurent qu'une précision de 10-bit
est réalisée pour le convertisseur de type pipeline. Les convertisseurs de type flash et pipeline présentés dans ce mémoire sont fabriqués sous les procédés CMOS de 0.25 et 0.18 micromètre, et les résultats démontrant leur opération réussie sont présentés.
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Chapter 1 - Introduction

1.1 - Motivation

The explosive growth of personal telecommunication system, video devices, disk drive, and automatic test equipments (ATEs) has created tremendous demands for analog-to-digital converters (ADCs) with high resolution, low supply voltage and low power consumption. To meet these demands, Nyquist-rate ADCs, such as flash and pipeline ADCs, have been the preferred architectural choice.

The resolution of the Nyquist-rate ADCs is limited by many factors, such as mismatch and noise. To improve the resolution, it typically requires an increase in either the die size, or the power consumption, or both. The increase in the die size and the power consumption is extremely undesirable since it will not be economical to manufacture or operate.

Low supply voltage poses another challenge in the design of the Nyquist-rate ADCs. The low supply voltage is demanded by most of personal telecommunication and portable device, where "AA", or "AAA" batteries are commonly used. Under the low supply condition, it would be even difficult to generate a band-gap voltage (~ 1.2 V). The band-gap voltage is used frequently in the ADCs. Alternative circuitries may be required to deal with the low supply voltage.

Besides the resolution requirement and the low supply voltage condition, power consumption is also crucial not only to portable device, but also to ATEs where a large
number of ADCs are employed in a single tester. By reducing power consumption, it would enable portable device to function longer time. And it would also reduce the cooling cost in ATEs.

With the above motivations, the goal of this research is to build high speed, low power, low voltage flash and pipeline ADCs in CMOS technology. The goal will be achieved with a digital DC reference source, which will be introduced in this thesis. It will be shown that the ADCs’s resolution is improved, while consuming no additional static power.
Monolithic Nyquist Rate ADC With Digital Calibration

Introduction

1.2 - Thesis Outline

This thesis is divided into six chapters. The first chapter introduces the motivation behind this work, as well as the organization of the thesis. Chapter Two provide a background study on the structure and operating principles of the digital DC reference source. Chapter Three focus on the design of a high-speed flash ADC. In the design of the flash ADC, the

Figure 1.1 Various application which requires analog-to-digital converter.
novel offset calibration algorithm will introduced. It will be shown that the proposed offset calibration algorithm not only reduces comparator offset, but also minimizes reference level mismatch in the flash ADC. Chapter Four deals with the design of a 10-bit one-bit per-stage pipeline ADC. In this chapter, the proposed offset calibration algorithm has also been adapted to reduce non-linear distortion induced by comparator offset. In addition, the proposed top-down design approach has been implemented in defining system level specification. It will be shown that this approach is reliable, and provides a well balanced separation between top-level and circuit-level design. In Chapter Five, the experimental results obtained from the flash ADC and the pipeline ADC will be presented and discussed. It will be shown that the proposed offset calibration algorithm is capable of improving the performance of flash ADCs and pipeline ADCs. The flash ADC is implemented in TSMC 0.25 μm CMOS process, and the pipeline ADC is implemented in TSMC 0.18 μm CMOS process. Finally, in the last chapter, a summary of the overall works will be presented, and future improvement will be proposed.
Chapter 2 - Programmable Digital DC Reference Source

2.1 - Introduction

A DC reference source is a common building block in mixed-signal microelectronic circuit. It can be found in various analog-to-digital converters (ADCs) and digital-to-analog converters (DACs). For instance, a flash ADC employs a number of highly correlated DC reference sources. In the case of a one-bit per-stage pipeline ADC, it utilizes a single DC reference source. As adopted in most ADCs and DACs, the DC reference source is required to be temperature independent, and insensitive to power supply noise and variations. To achieve this, traditionally, the DC reference source is implemented using band-gap reference source [1]. A band-gap reference source is capable of providing an output voltage on the order of +1.25 V, with a temperature coefficient in the range of 30-60 ppm/°C. Band-gap reference sources have been successfully implemented in bipolar, and CMOS processes where only lateral PNP transistors are available. However, as CMOS processes continues to improve and supply voltage continues to drop, it will be extremely challenging to design a band-gap reference source with a low supply voltage ( < +1.25 V ). Clearly, an alternative
implementation of a DC reference source will be needed.

![Figure 2.1 Typical band-gap reference source](image)

To resolve the difficulty of providing a constant reference voltage with a low supply voltage, a digital DC reference source [2] has been proposed recently. The proposed digital reference source does not require bipolar transistors. It can operate with supply voltage that are well below 1-V levels. In addition, the digital reference source can be digitally re-programmable in real time. These advantages lend itself well to the design of ADCs and DACs in a standard CMOS process.

In this chapter, the concept behind the proposed DC reference source will be introduced. First, it will be explained how DC reference generation is related to the signal processing operation that is performed. Once we establish that DC reference generation is just an extraction of a DC tone from an pre-designed signal, we will present the design strategies and circuitry in the actual extraction process. Finally, a set of complete analyses will be presented to show that the proposed DC reference source is temperature and power supply insensitive. In subsequent chapters, the proposed DC reference source will used in the design of a Flash and pipeline ADC.

### 2.2 - Theory

Unlike the band-gap reference source, the proposed reference source is based on a signal processing concept. From the view point of signal processing, a DC level can be regarded as a signal with a frequency of zero Hertz. If an arbitrary signal contains a DC tone of constant amplitude, the signal can be passed through a low-pass filter to extract its DC component. Ideally, the extracted DC tone can be used as a DC reference source.
The process of DC tone extraction is depicted in Fig. 2.2. As is evident, the key to generating a constant and stable DC reference source is a proper choice of the input signal and low-pass filter.

![Diagram of Signal Generation and Low-Pass Filter]

**Figure 2.2 The generation of a DC reference**

There are numerous signals which contain a DC tone of constant amplitude. In selecting an appropriate input signal for DC tone extraction, four criteria have been placed on the input signal: 1) It contains little low frequency signal content except the desired DC signal; 2) It is a digital and periodic signal; 3) It is easy to produce, store, and reproduce; 4) The amplitude of extracted DC tone is temperature and power supply independent. The first criterion is aimed to alleviate stringent demand on the low-pass filter. By choosing a signal with little low frequency signal content, the low-pass filter doesn’t require a low cut-off frequency to remove the unwanted low frequency content. Thus, the low-pass filter can be made small, and occupy little silicon area. The second criterion states a preference for digital signals over analog signals. Although both digital and analog signals can be used to encode DC tones, digital signals contain only two levels, "high" and "low", which is considered to be more "robust" than analog signals. In practice, the input signals are not only digital, but also periodic. Periodic digital signal can be implemented with limited amount of memory, while aperiodic signal can not. The third criterion is rather a qualitative requirement. With careful consideration, one can design circuits that generate, store, and reproduce the desired periodic digital signal with relative ease. In this chapter, \( \Sigma \Delta \) modulator has been chosen to generate the periodic digital input signal for DC tone extraction. Finally, the extracted DC level should not
drift with temperature variation, or change as supply voltage fluctuates. This criterion is crucial for any reference source. Any unwanted change in DC reference level would lead to performance degradation in ADCs. In this chapter, it will be shown that the ΣΔ modulator, combined with low-pass filter, possess a temperature coefficient and power supply rejection capability that is comparable to that of a band-gap reference source.

2.2.1 - Periodic Digital Signal (Digital Bitstream)

From previous discussions, we have arrived at the conclusion that a periodic digital signal is the preferred candidate for DC voltage reference generation. In this work, we shall commonly refer to the periodic digital signal as a digital bitstream. There are two forms of digital bitstreams that we are interested in: pulse width modulated (PWM) bitstreams and pulse density modulated (PDM) bitstream. In the following we shall demonstrated how a constant DC level can be encoded into each digital bitstream.

1. Pulse Width Modulated (PWM) Bitstreams

PWM bitstreams are widely used in industry for such applications as power supply generation, motor and various control systems. It is one of the simplest digital approach to encode a constant DC signal. The encoding is achieved by adjusting the duty cycle of each pulse of period T, as shown in Fig. 2.3. The duty cycle can be varied from 0% to 100%. For example, assuming each pulse has a height of $V_{ref}$, a duty cycle of 50% corresponds to a DC level of $\frac{1}{2}V_{ref}$, and 66.67% duty cycle corresponds to $\frac{4}{6}V_{ref}$.

![Figure 2.3 Counter based bit stream generation](image)
The PWM bitstream can be generated from a digital binary counter. The digital binary counter is typically implemented with a series of flip-flops. Depending on the states stored in the flip-flops, the duty cycle of each pulse can be set accordingly. For example, an 8-bit counter is capable of generating 256 different DC levels, corresponding to its 256 states.

![Figure 2.4 Conceptual Diagram of counter based PWM encoder](image)

2. Pulse Density Modulated (PDM) Bitstream

Unlike PWM bitstream, PDM bitstream encode a DC level by adjusting the density of pulses. A higher density of ones corresponds to a higher encoded DC level, and vice versa. An example of PDM bitstream is demonstrated in Fig. 2.5a, where PDM bitstreams corresponding to $1/2 V_{\text{ref}}$, $1/4 V_{\text{ref}}$, and $3/4 V_{\text{ref}}$ are shown. One of the more popular approaches in generating a PDM bitstream is to use a single-bit first-order $\Sigma \Delta$ modulator. The single-bit first-order $\Sigma \Delta$ modulator is shown in Fig. 2.5b. To encode a DC reference level, an accurate DC reference source is first presented to the input of the modulator. The modulator will then generate a corresponding PDM bitstream at its output at its clock rate.

The most significant advantage of this approach is that the $\Sigma \Delta$ modulator can be either implemented digitally on-chip in a standard CMOS process, or simply written in a piece of software. When implemented on-chip, a low-pass filter can be placed immediate after
the modulator to extract its encoded DC tone. However, when generated off-chip in software, the PDM bitstreams has to be first loaded into an on-chip memory, then passed through the low-pass filter to extract its encoded DC level. In this thesis, the software approach, combined with on-chip memory and low-pass filter, has been adopted for the generation of DC references in the operation of both the flash and pipeline ADCs. This approach at the time was considered to be less time consuming to implement, as only memory are required.

![Diagram](image)

(b) ΣΔ modulator

Figure 2.5 PDM streams with different DC level

2.2.2 - DC Tone Extraction

In Fig. 2.6 a complete implementation of the software-based programmable DC reference generator is presented. Here, the generator consists of a chain of D-flipflops (Size N) and an RC low-pass filter. The flip-flop chain acts as on-chip memory. To initialize the flip-flop chain, it is loaded with a software generated bitstream (PDM or PWM) containing the desired DC level. After initialization, the bitstream is cycled around in the flip-flop chain at a clock frequency \( f_s = 1/T_s \) to create a continuous periodic digital bitstream. The bitstream is passed through the RC low-pass, as shown in Fig. 2.6, to create a DC level. The time constant of RC filter is determined by the frequency contents of the bitstream.
As the bitstream is a pulse train, it contains frequency components other than DC. In particular, it contains AC tones that are integer multiplies of \( f_s/N \) as shown in Fig. 2.7, where \( N \) is the number of D-flipflop in the chain. It is therefore the objective of the RC low-pass filter to attenuate the AC tones to an acceptable level but allow the DC tone to pass unabated.

An RC circuit can be used to construct a first-order low-pass filter with transfer function

\[
H(s) = \frac{1}{sRC + 1}
\]
where $\omega_p = 1/RC$ is the pole frequency of the filter. As is evident from Eqn. (2.1), an RC-filter has unity gain at DC regardless of the value of R or C. However, as the bitstream contains frequency components other than DC, the RC filter will have an affect on the size of the AC components that pass through the filter. One can show that the RMS value of the AC tones that pass through the filter when they are all assumed to have equal amplitude of 1.0 V is given by

$$v_{\text{ripple - rms}} = \sum_{k=1}^{\infty} \frac{1}{\sqrt{2}} \cdot \frac{1}{N} \cdot \frac{1}{\sqrt{1 + \left(\frac{2\pi RCk^2}{N}\right)}}$$  \hspace{1cm} (2.2)

As it is evident from Eqn. (2.2), any change in the value of R and C will affect the magnitudes of AC ripple. Thus, by moderately over-designing the size of the R and C components will help to reduce the size of the AC ripples brought on by any variation in the absolute value of R and C. However, by choosing a large value for R and C, the convergence time to the desired DC level will be longer. A long convergence time may be unacceptable in some applications. In addition, by choosing a large value for R and C, more silicon area is also required. Careful consideration for selecting the size of R and C is therefore required.

2.3 - Analysis

As demonstrated previously, a digital bitstream followed by an RC low-pass filter is capable of generating an accurate and constant DC level. However, before adopting this approach for data converter applications, the strength and weakness of this approach should first be fully analyzed.

2.3.1 - Principles

The digital DC reference source consists of two components: a digital bitstream, and an RC low-pass filter. The digital bitstream encodes a DC reference in a sequence of 1-bit values and the low-pass filter extracts the DC reference from this bitstream.

The settling time, defined as the time that it takes for the RC filter to settle to within 10%
of desired DC level, is identical for both PWM and PDM bitstream. Furthermore, the settling time should be solely determined by the time constant of the RC filter. The settling of the output reference voltage, $V_{DC}$, can be expressed by Eqn. (2.3)

$$V_{DC}(t) = V_{DC\text{(final)}} \cdot \left(1 - e^{-t/(RC)}\right)$$

(2.3)

The effect of filter time constant is demonstrated in Fig. 2.8. The figure is obtained experimentally by feeding bitstreams into two RC filters with time constant of 16 ns and 160 ns. When tested with a time constant of 16 ns, the filter settles in less than 0.2 μs, but with an unwanted large AC ripple. When tested with a time constant of 160 ns, the filter settles in about 0.8 μs, but with a significantly reduction in the amplitude in AC ripples. With the settling time limited by the RC time constant, it is desirable to have as small AC ripples as possible. The minimization of AC ripples is possible by arranging frequency content of bitstream. PWM and PDM streams contains different frequency contents. It has been proven [2] that, for a given time constant, PDM bitstreams results in smaller AC ripples than PWM bitstream. For this reason, in this thesis, PDM bitstream generated from ΣΔ modulator has been used for DC level encoding. When it is used in A/D or D/A applications, a few micro-second start-up time should be allowed to ensure that the digital DC reference source is fully settled.
2.3.2 - Performance Measures

In most of applications, the digital DC reference source is implemented as shown in Fig. 2.6. Given that RC low-pass filter has been designed to attenuate AC ripples, digital information stored in the flip-flop chain is still susceptible to noise, temperature drift, and power supply fluctuation once it is converted into analog form.

- Noise analysis

In a digital DC reference source, multiple sources of noise exists. The most common sources of noises come from the power supply, substrate, and even within each transistor and resistor. In Fig. 2.9, three noise sources are shown that can have very different effects on the output reference voltage. Noise sources $n_1$ and $n_2$ originate from the flipflop chain. When $n_1$ and $n_2$ are passed through the low pass filter, the high-frequency noise content will be attenuated by the filter, and therefore will have less influence on the output level. The total amount of noise power present at the output due to $n_1$ and $n_2$ can be expressed as

$$P_{total} = f \cdot n_{BW} 
$$

where $f_{NBW}$ is the effective noise bandwidth and $H(s)$ is the transfer function of the RC
\[
V_{noise}^2(s) = \int_{0}^{\infty} |H(s)|^2 (V_{n1}^2(s) + V_{n2}^2(s))
\] (2.4)

low-pass filter.

However, the low-pass filter has little effect on the noise source \( n_3 \). This is due to the fact that noise source \( n_3 \) "sees" a high-pass filter, instead of a low pass filter. As noise source \( n_3 \) originates from the substrate, it usually can be minimized by implementing a guard ring around the RC low-pass filter.

![Figure 2.9 Noise sources and effect on the output level](image)

- **Temperature Analysis**

Critical to the operation of the DC generator is the area under each pulse of the bitstream. As the rise and fall times (\( T_{\text{rise}} \) and \( T_{\text{fall}} \)) of the flip-flops influence the shape of each pulse, it is important that these times are well-controlled and bounded values. As these times are dependent on temperature, several experiments were performed to determine the effect of temperature on the extracted DC level. The results are depicted in Fig. 2.10. Here, the results suggest that the average DC voltage has a temperature dependence of 288 ppm/°C in a temperature range of -5 °C to 100 °C.
Power Supply Sensitivity

For a DC reference, a high power supply rejection ratio (PSRR) is extremely desired. The proposed digital DC reference, when taken single ended, does not reject noise and voltage fluctuations in the power supply. This is quite evident, if one simply considers how a logical "1" alters that area under a single pulse.

Fortunately, the problem of low PSRR can be remedied. To increase PSRR, a differential digital DC reference source should be used. This is done by using an additional digital DC reference source to generate an "analog ground". The output is then taken with respect to the "analog ground" with another digital reference source. In this arrangement, any noise and fluctuation from power supply will show up in both DC reference source, and is rejected by the differential structure. By adopting differential digital DC reference source, an extremely high PSRR can be obtained. The differential digital DC reference source isn't implemented in this work. It is recommend as a possible future improvement.

2.4 - Conclusion

In this chapter, a digital DC reference source has been demonstrated, studied, and analyzed. The digital DC reference consists of only flip-flops and a RC low-pass filter.
It has been shown that the digital DC reference source is capable of generating arbitrary DC levels with constant amplitude. The temperature coefficient and power supply rejection ratio has been shown to be comparable to that of popular band-gap reference source. The proposed digital source has two advantages over the band-gap reference source: a) Low supply voltage (< 1.5), and b) Digitally programmable. Low supply voltage is significant in designing analog and mixed-signal circuitry for the advanced CMOS process, as the supply voltage will continue to drop in the CMOS process.

Programmability of the proposed DC reference is also significant in the design of ADCs and DACs. It allows for the possibility of changing DC levels in real time. This can then be used to compensate for circuit non-idealities, such as component mismatches. This feature of the proposed reference source will be fully demonstrated throughout Chapter 3 and 4, where a calibration algorithm has been developed that is centered around this DC reference source.
Chapter 3 - Flash ADC And Offset Calibration

3.1 - Introduction

Flash ADCs have always been a preferred approach for realizing very-high-speed analog-to-digital conversion. Flash ADCs continue to attract research interest [3] [4] due to the development of wireless networks, CCD image device, and high-speed automatic testing equipment (ATE). These research interests are mainly focused on realizing high-speed flash ADCs in standard CMOS process, as to reduce the cost and increase the level of system integration.

Flash ADCs offer unparalleled speed as compared to other Nyquist rate ADCs such as successive approximation, pipeline, or folding-interpolation ADCs. A 6-bit CMOS flash ADC with a sampling rate over 1 GHz [5] has been reported. However, there are numerous challenges in designing a multi-GigaHertz high-resolution flash ADC. These challenges includes how to minimize mismatch in the reference levels and reducing variation in comparator offset. In this chapter, these design challenges will be addressed. Design recommendations will be proposed. These recommendations include the adoption of digital DC reference sources described in Chapter Two. These DC sources will be used to improve the matching of the reference levels. In addition, a novel comparator offset calibration algorithm has been developed with the use of the digital reference source. The
offset calibration algorithm is capable of reducing variation in the comparators offset to less than ±1/2 LSB. Experiments have been conducted that demonstrate significant performance improvement in flash ADCs.

In this chapter, the proposed flash ADC will be discussed in detail. The flash ADC implemented in this work is meant to demonstrate the capability of the programmable DC source for improving the performance of flash ADCs. It has not been optimized for area or power. However, it will be shown that, as the CMOS technology continues to improve, the silicon area of the proposed flash ADC will scale down significantly in size. Future improvements have also been proposed which could significantly reduce area and power consumption.

The proposed flash ADCs prototype have been built using discrete components, and tested with a mixed-signal tester at McGill University. The results of these tests will be provided and discussed in Chapter Five.

3.2 - Flash ADCs Theory and Analysis

Traditional flash converter, as shown in Figure 3.1 in block diagram form, consists of a voltage reference generator, a comparator bank, and a digital encoder. During its normal mode of operation, an input signal, \( V_{in} \), is sampled and held by a track/hold (T/H) circuit. The sampled input is then compared to each of the reference voltage levels \( v_1, v_2, ..., v_N \) simultaneously, hence the name “flash”. As a result of the comparisons, a thermometer code is generated. The thermometer code is then converted into a binary code by a digital encoder after each clock cycle.

For an \( n \)-bit flash ADC, \( 2^n \) reference levels and comparators are required. The comparator bank generates \( 2^n \) different thermometer codes (from 00...0 to 11...1). The digital encoder converts the thermometer codes into \( 2^n \) \( n \)-bit wide binary codes. The operation of the flash ADCs is straight forward. A simplified implementation of a 3-bit flash ADC is shown in Figure 3.2, where the voltage reference generator is implemented with a string of identical resistors.
Most of flash ADCs are designed for high-speed applications (100 MHz and above). During high-speed operation, flash ADCs are extremely sensitive to temperature drift, mismatches, and process variation. In order to meet the high-speed requirement, design limitations and circuit non-idealities must be well understood.

Major performance limitations include clock jitter, reference levels variation and comparator offset variation. Clock jitter affects the input signal sampling accuracy and raises the noise floor in the converted signal. Variation in reference levels and comparators offset induces DNL and INL errors, which are a form of non-linear distortion. There are other factors which could also affect the performance of flash ADCs, especially when the ADCs are designed for a higher speed applications (1.0 GHz and above). These effects will be described in later sections.

In addition to the performance limitation mentioned above, physical limits exists that can hinder the implementation of high-speed high resolution flash ADCs. Physical limitation becomes apparent as ADCs' resolution increase beyond 8 bits. The number of reference levels and comparators grows exponentially as the resolution increase. Since the reference voltage are derived from a resistor string, the number of resistors will also increase exponentially. The exponential growth of resistors and comparators could consume a large silicon area. However, in recent years, a large demand for high-speed high resolution flash ADCs come from applications such as radar system, satellite receiver, and ATEs. The manufacturing cost of Giga-Hertz flash ADCs (i.e. 8-bit 1.5 GSPS MX-104 from Maxim and 10-Bit 1.0 GSPS RAD020 from Rockwell) is negligible as compared to their retail
price ($200 ~ $500). Thus, silicon area is not a constraint and a large amount of comparators can be placed on chip. This is an important development as it may be possible to design flash ADCs with even higher resolution in the Giga-Hertz range.

3.2.1 - Clock Jitter

Typical high speed flash ADCs contain sampling circuits, which are used to relax settling time requirement on the comparators. The most popular implementation of the sampling circuit is a track/hold (T/H) circuit. In ADCs implementations, the T/H circuit is driven by a clock generated from the input clock driver, as shown in Fig. 3.3. The clock jitter, induced in the input clock driver, will directly affect T/H sampling points in time, thus degrading SNR of sampled signal. For high speed ADCs, every effort should be made to reduce clock jitter.
Clock jitter is one of the major sources of error which degrade the performance of flash ADCs. Clock jitter refers to small random movement of clock edge with respect to a given clock edge. In an A/D system, the small random movement of clock edge result in an inaccurate sampling of input signal as show in Fig. 3.4

To show the effect of jitter on the Track and Hold (T/H) circuitry, one can assume that an ideal sine wave, \( f(t) = A \sin(2\pi f_0 t) \), is sampled with a jittery clock. The clock has an RMS value of jitter \( T_{j,\text{rms}} \). The performance of T/H circuitry (SNR) is solely determined by the RMS power of clock jitter and the frequency of the input signal[6][7]. SNR is given as

\[
SNR = 20 \cdot \log \left( \frac{V_{\text{in} - \text{rms}}}{V_{j - \text{rms}}} \right) \\
= 20 \cdot \log \left( \frac{A/\sqrt{2}}{2\pi A f_0 T_{j - \text{rms}}/\sqrt{2}} \right) \\
= -20 \cdot \log \left( 2\pi f_0 T_{j - \text{rms}} \right)
\] (3.1)
where $V_{\text{sin-rms}}$ is the RMS value of the input sine wave, $V_{\text{j-rms}}$ is jitter-induced sampling error, and $f_o$ is the input sine wave frequency. In Fig. 3.5, an input sine wave with amplitude $A = 1$ is being sampled by a clock with 1 ps, 4 ps and 10 ps (RMS) jitter, a set of achievable SNR are plotted. For example, if an input sine wave of 100 MHz is sampled with 10 ps jitter clock, the highest achievable SNR is at most 43 dB (assuming the input sine wave is sampled at least at Nyquist rate).

![Jitter vs SNR](image)

Figure 3.5 Jitter vs. SNR for an ideal sample system

### 3.2.2 - Reference Levels Mismatch

Beside clock jitter, reference levels mismatch is another major source of error. Reference levels mismatch will leads to DNL and INL errors. In this section, it will be shown how resistors mismatch can result in DNL and INL error in flash ADCs.

Ideally, for a n-bit flash ADC, there are $2^n-1$ reference levels, denote here as $V_1, V_2, \ldots, V_N$, (where $N = 2^n-1$). A common approach of generating the reference levels is to apply the voltage generated by a band-gap reference across a string of identical resistors. Assuming there is no mismatch in resistance, a voltage of $\Delta v$ should appear across each resistor. In practice, however, some mismatch will exist on account of variations in doping profile, geometry and temperature gradients across the die of the chip. Thus, each
reference voltage generated by the resistor string deviates from an ideal reference voltage resulting in a transfer characteristic that deviates from the idea, as shown in Fig. 3.6.

Each generated reference voltage is a function of all resistors in the resistor string. The reference voltage, $V_i$, can be described as

\[
V_i = \frac{\sum_{n=1}^{N} R + \Delta R_n}{2^N + 1} \cdot V_{ref}
\]

where $R$ is the mean of all the resistors in the resistor divider network, $\Delta R_n$ is amount of deviation of the $n$th resistor from the mean value ($R$). There are $2^N + 1$ number of resistors in the string. To obtain DNL and INL, a straight line approximation [7] is typically used. Straight line approximation usually results in both offset and gain error, which can corrected digitally. By ignoring offset error and gain error, DNL and INL of the Flash ADC can be related to the $\Delta R_n$ according to the following:

\[
DNL[i] = \frac{V_{ref}}{(2^N + 1) \cdot R} \cdot \sum_{n=1}^{i} \Delta R_n
\]

\[
INL[i] = \sum_{m=1}^{i} DNL[m] = \frac{V_{ref}}{(2 + 1) \cdot R} \cdot \sum_{m=1}^{i} \sum_{n=1}^{m} \Delta R_n
\]

Figure 3.6 Effect of resistor mismatch on DNL and INL
As is evident from Eqn. (3.3) and Eqn. (3.4), to minimize DNL and INL, it is imperative to ensure that the variable, ΔR, is small. However, the variable ΔRn is a complex function of resistance, geometry, and fabrication process. Minimization of ΔR is usually done by careful layout, resistor averaging technique and laser trimming [8][9]. These approaches are either limited, or, in the case of laser trimming, expensive to implement in practice. In this thesis, a novel approach, with the help of the digital reference source introduced in Chapter Two, will be used to minimize the effect of ΔR. This approach is fully digital and is capable of reducing the effect of ΔR to a controllable level. The approach will be discussed in some detail in Section 3.2.4.

3.2.3 - Comparator Offset Variation

The comparator shown in Fig. 3.7 is also one of the most crucial components in a Flash ADC design. It is probably the most difficult component to design in a flash ADC, as the comparator is required to have small static and dynamic offset (< 1/2 LSB) and small offset variation from comparator to comparator. In this subsection, the sources of the offset will be explored and a remedy will be proposed.

![Figure 3.7 A common latched comparator with output buffer](image)

The main source of comparator offset stems from transistors mismatches. For example, in a simple latched comparator shown in Fig. 3.7, a mismatch in transistor threshold voltage...
and transconductance can induce as much as 30-70 mV offset when operating from a 3.3 V supply. The mismatch in CMOS transistor were studied and characterized in [10]. Here a simple square-law relation was used to characterize the transistors,

$$I = \frac{K}{2}(V_{GS} - V_T)^2$$  \hspace{1cm} (3.5)

The deviation in both $V_{TH}$ and $K$ were derived and verified. In the case of transistor threshold mismatch, its variation can be formulated as

$$\sigma^2_{VT} = \frac{1}{LWC^2} [q(Q_B + Q_f + qD_I) + A_{ox}(Q_B + Q_f + q^2D_I^2)]$$  \hspace{1cm} (3.6)

where $\sigma_{VT}$ is standard deviation of threshold voltage, parameters $L$, $W$ and $C$ are the transistor length, width, and channel capacitance, respectively, and parameters $Q_B$, $Q_f$, and $D_I$ are the transistor depletion charge density, fixed oxide charge density, and threshold adjust implant dose, respectively. $A_{ox}$ is a experimentally measured parameter. As it is evident from Eq. (3.6), transistor matching improves as the area of transistor increases.

In a similar manner, the standard variation of the transistor gain, $K$, was described with the following formula,

$$\frac{\sigma^2_K}{K^2} = \frac{1}{LW}(A_\mu + A_{ox}) + \frac{\sigma_L^2}{L^2} + \frac{\sigma_W^2}{W^2}$$  \hspace{1cm} (3.7)

Here $A_\mu$ is experimentally measured parameters, and $\sigma_L$ and $\sigma_W$ are the standard deviations of the actual transistor length and width ($L$ and $W$). Once again, it illustrates that the larger the product of $L$ and $W$, smaller the mismatch between transistors.

From the above study, two conclusions can be reached: 1) By increasing the product of $L$ and $W$ (effective area) the mismatch between transistors can be reduced, and 2) N-channel transistors have better matching properties than P-channel transistors, as $K$ is larger with an NMOS device of the same dimension. However, it is not always desirable to select a large $L$ and $W$. A large $L$ and $W$ will result in a large comparator input capacitance, which translates to either higher power consumption, or reduced bandwidth. Essentially, there is a physical limit on how closely transistors can be matched in a given CMOS process. To
overcome this limitation, an on-chip calibration algorithm has been developed. The details of this offset calibration technique is presented next.

3.2.4 - Digitally Calibrated Comparator

As described in the previous section, process insensitive designs call for the judicious use of large NMOS transistors at the expense of high power consumption and reduced bandwidth. Clearly, a new method is needed that does not compromise the power and speed requirements. Of course, the technique should be immune to process variations, otherwise we would have come full-circle. Towards this end, we propose the Digital Calibrated Comparator (DCC) circuit shown in Fig. 3.8. At the center of the DCC design is the DC reference generator described in Chapter 2. During DCC operation, the D-flip-flops are initialized and loaded with a predefined bit stream pattern containing the desired DC level. As explained in Chapter 2, the DC level can be encoded in either PWM or PDM format. After passing a repetitive sequence of the programmed bit stream through a simple low-pass filter (RC filter), a DC tone is extracted and converted to a analog voltage level that resides at the input to the comparator. Through the control of the appropriate 1-bit digital sequence, the DCC can correct for device mismatches and process shifts by altering the DC level set at one input terminal of the comparator.

![Digital DC reference generator](image)

Figure 3.8 The proposed DDC, using the digital DC reference generator.

A novel flash ADC implementation consisting of only DCCs is shown in Figure 3.9. In essence, the DCC has replaced the resistor-string / comparator combination in Figure 3.2
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with a process insensitive design. In the next section, the detailed implementation and analysis of the novel flash ADC will be discussed.

The advantages of the DCC over the existing resistor-string-comparator combination in a traditional flash ADC is as follows:

1) The DCC is insensitive to RC matching

2) The DCC is digitally re-configurable, therefore making itself suitable for a wide range of input signal levels without pre-amplification or scaling, and

3) The DCC can be configured to eliminate comparator offset (both static and dynamic offset).

- Digital Calibration of Comparator Offset

A flash ADC contains a bank of clocked latched comparators. The typical clocked latched comparator in Fig. 3.7 contains both an input differential pair and a regenerative feedback circuit. Due to process variations, mismatch between the input differential pair (\(M_1\) and \(M_2\)) will occur. The mismatch results in unbalanced current distribution within its two branches that then leads to a static offset. Dynamic offset is also caused by transistor mismatches, but happens only in the latch stage during the clock transition from high to low. During this transition, the currents \(I_1\) and \(I_2\), induced by the charge injection from \(M_7\),
flow into transistors $M_3$, $M_4$, and $M_5$, $M_6$. Under general conditions, the impedance looking into the node_1 and node_2 are different due to transistor mismatches. Therefore, $I_1$ and $I_2$ are unequal. The difference in the injected current $I_1$ and $I_2$ cause a common mode jump in the comparator’s output, $Q$ and $Q_n$, which leads to the dynamic offset.

![Diagram](image)

**Figure 3.10** Cause of dynamic offset, due to mismatch and charge injection

To achieve higher than 6-bit resolution for a flash ADC, without trimming, some form of calibration is required. The calibration process generally involves two steps: 1) measurement, and 2) correction. The proposed DDC is fully capable of performing both measurement and correction. In Figure 3.11, the comparator is modeled as an ideal comparator with an offset component, $\Delta V_{\text{offset}}$. The proposed voltage reference generator, $V_{\text{cal}}$, is connected to negative terminal of the comparator, and an ideal voltage source $V_{\text{ref}}$ is connected to the positive terminal of the comparator. Assuming initially $V_{\text{in}} > V_{\text{cal}}$, the output of the comparator will be 1. To begin the calibration process, $V_{\text{cal}}$ is programmed to increase linearly. This is accomplished by loading it with bitstreams representing increasing DC values. When $V_{\text{cal}} \geq V_{\text{ref}}$, a transition of from 1 to 0 at the output will occur. The voltage, $V_{\text{cal}}$, which caused the transition is called the Calibrated Reference Voltage, which contains both the ideal reference voltage and $-\Delta V_{\text{offset}}$. During normal operation of the flash ADC, the input signal $V_{\text{in}}$ is connected to the positive terminal. Since the Calibrated Reference Voltage contains both the ideal reference voltage and -
ΔV_{\text{offset}}, the voltage -ΔV_{\text{offset}} will cancel out with +ΔV_{\text{offset}} present in the comparator model. Therefore, the input signal is theoretically being compared only to the ideal reference voltage.

![Figure 3.11 Behaviour model of the comparator and calibration process](image)

The digital calibration process, for the proposed flash ADC, is described in Figure 3.12. V_{\text{ref(n)}} is the ideal reference voltage for the nth comparator. Q(n) is the output of the nth comparator. B(m) is the mth DC tone bitstream which caused the transition of 1 to 0 at the comparator output (total number of DC tone bitstreams should be at least 2N).

The digital calibration process generates a bitstream which not only contains an ideal DC reference, but also compensates for the comparator offset (both static and dynamic). The calibration process is required only to run once at start-up. For a 10-bit flash ADC, the calibration process takes at most \(2^{10} \times 10 \text{ ms} = 10.24 \text{ s}\).
a) Basic topology

b) Close switch $S_1$ and load DC generator with bitstream $B(0)$ which contains DC level of $V_{CC}/N$.

c) Different DC bitstreams are loaded until $Q$ change from 0 to 1. Record the bitstream $B(m)$ which caused transition

d) Open switch $S_1$ and close Switch $S_2$. Stage $n$ is fully calibrated.

Figure 3.12 Calibration steps
3.3 - Implementation Issues

3.3.1 - Comparator Design

In the design of high-speed flash ADCs, there are two major challenges in choosing a suitable comparator architecture. First, comparator offset must be within a certain limit (i.e., < ±1/2 LSB) determined by resolution of the flash ADC. A large comparator offset would result in non-linear distortion, or even lost quantization levels. Fortunately, the proposed DCC is capable of reducing the comparator offset to an acceptable level. The second challenge is to minimize the variation in the comparator response time (delay), thus minimizing meta-stability. The comparator response time must not exceed a pre-defined amount of time \( T_s / 2 \), where \( T_s = 1 / F_s \). A large variation in comparators response time would cause a set of incorrect thermometer codes to be latched and therefore result in conversion errors (also refer to as “bubble” errors).

As it is apparent from Fig. 3.10, once the “Latch” signal turns off, the latched comparator will require some time to settle. This settling time will be determined by the dominant pole of the regenerative feedback circuitry. The latched comparator is essentially unstable, which is due to the existence of a dominant positive pole. The dominant positive pole of the latched comparator is given by [13]:

\[
P_{pos} = \frac{g_{m_{NMOs}} + g_{m_{PMOS}}}{C_{d_{NMOs}} + C_{d_{PMOS}}}
\]

Eq. (3.8) shows that the settling time of the comparator is determined by the \( g_m \) of the transistors \( (m_3, m_4, m_5, \text{ and } m_6) \) in Fig. 3.7. It can also be shown that delay of the latched comparator can be expressed as [13]

\[
T_{delay} = \tau \cdot \ln(2) = 0.68 \cdot \tau
\]

where \( \tau \) is equal to \( 1 / P_{pos} \). The \( g_m \) of the transistors is a function of the input signal, biasing current, and transistor aspect ratio (W/L). The dependence of \( g_m \) on the input signal can be quite problematic. At any moment in a flash ADC, the value of the input signal is always close to some references, and far away from the others. The comparators
which "see" two similar voltage could have large delay, while the others can have small delay. This phenomenon is referred to as "dispersion" and is demonstrated through Hspice simulation shown in Fig. 3.13. In Fig. 3.13, an input signal is compared to 1.25 V. It can be seen that, the comparator delay is larger as the input signal is closer to 1.25 V. Dispersion is inherent in all flash ADCs. Further Hspice simulation have revealed that comparator delay is approximately inversely proportional to the input voltage. These simulation results are shown collectively in Fig. 3.14, where the comparator delay is plotted against the input signal strength.

One simple solution to reduce the comparator delay is to increases the biasing current, $I_D$, as shown in Fig. 3.7. Intuitively, by increasing the biasing current, the charge can be either removed or deposited in drain and gate capacitance of the transistor $m_3$, $m_4$, $m_5$, and $m_6$ at a faster pace, thus causing the transistor $m_3$, $m_4$, $m_5$, and $m_6$ to either switch on or off at a faster pace too.
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Figure 3.13 Hspice simulation of comparator delay with various input signal

Figure 3.14 Comparator delay as input voltage
Another common approach is to use an additional pre-amp stage, which consists of a differential pair with resistive load. The pre-amp stage is limited to have a small gain (5 ~ 10 V/V) as to ensure a maxim bandwidth. By adding a pre-amp stage with a hard upper and lower limit, the input signal will be amplified before being presented to the latched comparator. Thus each comparator will see an amplified input signal, which has roughly the same range of amplitude, thereby eliminating the variable comparator delay.

In the design of proposed 4-bit flash ADC, we opted for the simpler approach of increasing the current biasing to get around the comparator delay problem. To remind our readers, the goal of this work is to demonstrate the reference level correction and offset calibration algorithm, rather than create a low power flash ADC.

In the design of the proposed 4-bit flash ADC, the comparator has the architecture depicted in Fig. 3.15, which is slightly different from the comparator shown in Fig. 3.7. The regenerative PMOS latch in Fig. 3.7 is replaced with a static pull-up network (M, M7, M8 and M9). The static pull-up is biased by a dedicated biasing circuitry, and is capable of pulling a large amount of current during latching up, thus increasing the response time of the comparator.
NMOS transistors $M_1$ and $M_2$ have an aspect ratio of $W/L = 24 \mu m / 0.5 \mu m$, the PMOS transistors $M_5$, $M_6$, $M_7$, and $M_8$ have an aspect ratio of $W/L = 60 \mu m / 0.5 \mu m$, and NMOS transistors $M_9$ and $M_{10}$ have an aspect ratio of $W/L = 4.8 \mu m / 0.25 \mu m$.

Hspice simulation have been performed on the comparator to determine the variation in comparator delay. The comparator delay is regarded as a function of biasing current. The simulation results are shown in Fig. 3.16 demonstrates that, as the biasing current decreases, the delay increases as well. And furthermore, Fig. 3.17 indicates the comparator delay is inversely proportional to the biasing current. Therefore, it can be concluded that the reduction in the comparator delay can be achieved with a large biasing current, however at the expense of a higher power consumption. In the design of the proposed 4-bit flash ADC, a biasing current of 100 $\mu$A is chosen such that for an input voltage of 0.01 V, the comparator delay is designed to be 1.25 ns. A 1.25 ns delay ensures a performance of 4-bit resolution up to 800 MHz. Above 800 MHz, the bubble error starts becoming the dominant source of error and degrades the performance of the flash ADC.
Figure 3.16 Hspice simulation of comparator delay with various biasing current

Figure 3.17 comparator delay vs biasing current, with $V_{in} = 0.01 \text{ V}$
3.3.2 - D Flip-Flop Chain

The proposed flash ADCs stores digital bitstreams on-chip, which are used for DC generation and calibration purposes. The bitstreams are stored in a chain of flip-flops. Each flip-flop is implemented as a master slave latch, as shown in Fig. 3.18. The master-slave latch utilizes two-phase non-overlapping clocks.

![Figure 3.18 Master-slave latch used to store digital bitstreams](image)

The flip-flop chains are designed to work in two modes: 1) Stream_In mode, and 2) Recycle mode. The mode of operation is determined by a front-end multiplexer shown in Figure 3.19. When the flip-flop chain is engaged in one of the two modes, the other mode is disabled. Stream_In mode is used during the start-up phase of the flash ADC. In Stream_In mode, a digital bitstream is loaded into the flip-flop chain. During normal operation of the flash ADC, the flip-flop chain is in Recycle mode, where the bitstream is cycled through the chain continuously.
Figure 3.19 Flip-flop chain with two modes of operation.

As discussed in Chapter Two, the magnitude of AC ripples which is riding on top of the DC level is determined by the time constant of RC low-pass filter and clock speed of the flip-flop chain. With higher clock rates, the frequency of the ripple is located in a higher frequency band, thereby allowing an RC low-pass filter with a smaller time-constant. This is beneficial because a smaller on-chip resistor and capacitor combination is required, hence, less silicon area is necessary. The higher clock rate is only achievable with a faster flip-flop. The flip-flop, shown in Fig. 3.18, has to be sized properly, in order to achieve high speed operation. In the design of the proposed flash ADC, using the TSMC 0.25 μm CMOS process, the NMOS is sized to a W/L = 1.0 μm / 0.5 μm, and PMOS is sized to a W/L = 1.2 μm / 0.5 μm. By adopting such aspect ratios, a rise time of 800 ps and fall time of 300 ps can be achieved. The flip-flop chain can be operated at a maximum clock rate of 333 MHz. Hspice simulation shown in Fig. 3.20 demonstrate that the flip-flop operates comfortably at a clock rate of 200 MHz. This was deemed sufficient for DC reference generation with a R & C of 100 KΩ & 5.0 pF values, respectively.
3.3.3 - Clock Driver

In the design of the proposed flash ADC, the flip-flop chain has a length of 1024 bits. In each flip-flop, the clock driver must be able to drive four gates, two outputs connected to $\phi_1$ and two connected to $\phi_2$. The total gate capacitance for each flip-flop is 16 fF, which means the entire flip-flop chain has a total gate capacitance of 16 pF. The clock driver is used to drive the flip-flop chain, therefore a clock rate of 200 MHz will suffices.

The clock driver is designed to generate a two phases non-overlapping clock, which is capable of driving 16 pF of capacitive load. The clock driver is shown in Fig. 3.21. The Hspice simulation results, shown in Fig. 3.22, confirms that the clock driver indeed generates a two phases non-overlapping clock.

![Clock Driver Diagram](image)

**Figure 3.21 Two phases non-overlapping clock driver**

![Transient Response Graph](image)

**Figure 3.22 The generated two phases clock, with 16 pF load at 200 MHz**
3.3.4 - Layout

To prove the concept of the digitally programmable DC reference source and offset calibration algorithm, a 4-bit flash ADC has been implemented in TSMC 0.25 μm CMOS process. The micrograph of the flash ADC is shown Fig. 3.23, where an area usage breakdown is given in Table 3.1.

As it is evident in Fig. 3.23, the majority of the area is used for the D-flipflop chain. For sixteen 1024 flip-flop chains, an area of 3.12 mm² is required. The implementation is known to be area inefficient, but sufficient for proof-of-concept. Another major area consumption is from the on-chip RC low-pass filter, which occupies an area of 1.09 mm². In this implementation, there are 16 RC low-pass filter, each RC low-pass filter consists of a 200 kΩ resistor and a 6 pF capacitor (τ = 1200 ns). The RC filters were over-designed to minimize the ripple at the output of the proposed DC reference source, given a 20 MHz clock rate. There are various techniques to minimize the area consumed by both the D-flip-flop chains and the RC filters. The techniques include using on-chip PLL source, asynchronous flip-flops, standard ROM memory, and micro-processor controlled single RC filter implementations. These techniques will be discussed in detail in the next section.

<table>
<thead>
<tr>
<th>Component</th>
<th>Area (mm²)</th>
<th>Area (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Clock Buffer</td>
<td>0.408</td>
<td>7.08</td>
</tr>
<tr>
<td>Flip-flop Chain</td>
<td>3.12</td>
<td>54.2</td>
</tr>
<tr>
<td>RC</td>
<td>1.0944</td>
<td>18.9</td>
</tr>
<tr>
<td>Comparators</td>
<td>0.0484</td>
<td>0.84</td>
</tr>
<tr>
<td>Misc.</td>
<td>1.00</td>
<td>17.4</td>
</tr>
</tbody>
</table>

Table 3.1: Area of 4-bit Flash ADC (Total area 5.76 mm²)
3.4 - Future Improvements

The main disadvantage of the proposed flash ADC is area inefficiency. Fortunately, the area inefficiency can be remedied by adopting several advanced digital techniques. It should be noted, however, there are two significant reasons behind utilizing the proposed digitally programmable DC reference source. First, DC reference generation using digital bitstreams is considered to be more robust than a pure analog approach. Second, the silicon area dedicated to digital circuits scales as the silicon fabrication process continues to improve. This trend is evident from Table 3.2 where minimum transistor geometry has been shrinking continuously. It is predicted, by 2014, the minimum transistor will have a length 0.035 μm. Therefore, it is definitely worthwhile to improve the existing architecture implemented in this chapter. The possible improvement includes standard DRAM memory and micro-processor controlled single RC filter implementation. It will be shown that the proposed improvement can drastically reduce the area required for a flash ADCs.
3.4.1 - Standard DRAM Implementation

The main purpose of the D-flipflop chain is to store the digital bitstream, which contains in coded form the desired DC reference level. A DRAM can also be used to perform this same function. The conceptual design of a flash ADC using standard DRAM is shown in Fig. 3.24.

There are two major advantages for adopting a DRAM approach. First, existing DRAM densities can be made extremely high. For an 8-bit flash ADC, there are 256 different voltage reference levels required. Each voltage level requires a D-flipflop chain with a length of at least 1024 bits. The total number of bits required for such a flash ADC would be $1024 \times 256 = 256$ Kbits. According to Fig. 3.25, by 2010, if standard DRAM is used, the area occupied by 256 Kbits only amounts to $0.1 \text{ mm}^2$, which is negligible compared to the area required if D-flipflop are used. The second advantages stems from the architecture of the standard DRAM. Data stored in the DRAM is best accessed in blocks. For a 8-bit flash ADC, during each clock cycle, 256 bits are required to be retrieved from the DRAM, and sent in parallel to the RC network. Such a block access can be achieved within an approximate time of 10 ns [16]. This is equivalent to cycling the data stored in a D-flipflop chain at a clock speed of 100MHz. Since the size of RC low-pass filter is also a functions of clock rate, the values of R and C can be reduced, thereby reducing the amount of silicon area required.

The standard DRAM approach can significantly reduce the silicon area dedicated to store the DC encoded level. The standard DRAM approach is a complete digital approach, which will scale down in size and speed up as the silicon fabrication technology continues to improve in the near future. However, this approach still requires 256 RC low-pass
filters; a dominant source of area consumption. Further reduction in area consumption is possible, which leads us to the next approach.

Figure 3.24 Proposed DRAM Flash ADC

Figure 3.25 Trends in DRAM chip area and wafer area. 1997 data from ISSCC, VLSI Circuit Symp. [16]

3.4.2 - Micro-processor Controlled Single RC Filter Implementation

To further reduce the size of the DC calibrated flash ADC, one must consider reducing the size of the RC filter bank. One scheme would be to use a single RC low-pass filter to filter a set of DC encoded bitstreams and store the various DC levels in a bank of capacitors as depicted in Fig. 3.26. The advantages of this scheme is that a large reduction
in silicon area results, as only one RC low-pass filter is required, even though a capacitor bank has to be added. Fortunately, the capacitor bank can be constructed from a set of small sized capacitors.

The actual capacitor size will depend on the length of time the DC level is expected to be held for. Any change in the amount of charges stored in the capacitors will be reflected on the DC reference levels, hence, the resolution of the flash ADC. In the capacitor bank, each capacitor is connected to at least two switches which permits the charging and holding actions to take place during each clock cycle. It can be shown, as depicted in Fig. 3.27, that the charge stored in the capacitors will slowly leak into the substrate. The leakage occurs through the reverse-biased diodes, D1 and D2. The amount current leaked into the substrate is known as the leakage current, $I_s$, which is in the order of $10^{-9} \sim 10^{-15}$ A.

The size of the capacitors in the capacitor bank is determined by both the leakage current $I_s$ and the resolution of the flash ADC. For example, given a capacitor of size $C$, which stores $Q$ amount of charge, will develop the following voltage across the capacitor

$$V_c = Q \cdot C$$

After time $T$, amount of charge leaked out of the capacitor $C$ is $Q_{\text{left}} = I_s \cdot T$. Therefore, the change in the voltage across the capacitor is

$$\Delta V_c = (Q - 2 \cdot I_s \cdot T) \cdot C$$

The value of $\Delta V_c$ is determined by the resolution of the flash ADC. In order to achieve $N$-bit resolution, at time $T$, $\Delta V_c$ has to be less than $\text{LSB}/2$. Therefore, for a $N$-bit flash ADC, the following equation must be satisfied at time $T$

$$\frac{C \cdot V_c - 2 \cdot I_s \cdot T}{C} < \frac{\text{LSB}}{2}$$

In Eq. (3.12), the variable $T$ and $C$ are inter-related. The time $T$ is the minimum interval which the capacitors in the bank has to be refreshed. A larger time interval would require larger capacitors in the bank, which holds more charges. For a typical 8-bit flash ADC, the
value of each capacitor in the bank is chosen to be 0.5 pF. In the worst case, where \( V_c = \text{LSB} \), then

\[
2 \cdot I_s \cdot T < \frac{\text{LSB}}{2} \\
T < \frac{\text{LSB}}{4 \cdot I_s}
\]

(3.13)

If the 8-bit flash ADC has an input range of \( V_{\text{range}} \) (i.e. 3.0 V), then \( \text{LSB} = \frac{V_{\text{range}}}{2^8-1} = 0.0117 \text{ V} \). Using Eq. (3.13), the minimum time interval, \( T \), required to refresh the capacitors is found to be 2925000 s, or approximately 33 days. The refreshment of each capacitor in the bank is done by a micro-processor as shown in Fig. 3.26.

The overall operation of the micro-processor controlled flash ADCs can be divided into two phases: 1) start-up and offset calibration, and 2) normal operation and reference refreshment. During the start-up phase, the micro-processor retrieve each appropriate bitstream from the DRAM, then feed the bitstream to the RC filter. The output of the RC filter, \( V_{\text{out}} \), charges a corresponding capacitor in the capacitor bank. The final voltage stored in each capacitor should account for both a desired reference voltage and an offset compensation voltage. Once all the capacitors in the capacitor bank are charged, the flash ADC is ready for the normal operation. During normal operation, the comparators makes decisions based on the input signal and reference voltages stored in the capacitor bank. Furthermore, the capacitors in the banks are required to be refreshed once every few minutes in order to minimize the charge loss. This refreshment process is coordinated by the on-chip micro-controller.

It should be self-evident that the entire flash ADC contains only two analog components: an RC filter and a set of comparators. The rest of circuits are standard digital circuits, and can be easily designed with software package such as VHDL or Verilog. The advantages of the adopting digital circuitry in the flash ADC should be more obvious in the future as the digital circuitry continues to scale down in size.
3.5 - Conclusion

In this chapter, the design and implementation of a 4-bit flash ADC has been studied. The study reveals that incorporating a digital reference generator into the architecture of the ADC, it is possible to minimize two common error sources: reference level mismatch and comparator offset. Furthermore, several alternative architectures were proposed that simplify the digitally-calibrated designs even further.
Chapter 4 - Multi-Step ADCs

4.1 - Introduction

With the emergence of cable modem, DSL and hand-held communication devices, there is a strong demand for Nyquist rate analog to digital converters (ADCs) which provide a moderate resolution with a reasonable bandwidth and power consumption. Multi-step ADCs, with a typical resolution of 10 to 12 bit, a power consumption in the range of 20 to 200 milliwatts and a sampling rate of up to 20 MSample/s, have been becoming a favorite choice of architecture.

Multi-step ADCs belong to the class of Nyquist-rate ADCs, which can theoretically convert an analog signal into a digital representation at a rate of up to $F_s/2$, where $F_s$ is the ADC sampling frequency. This is achieved by utilizing multiple stages, where each stage handles a portion of the overall conversion process. Each stage typically contains a low-resolution ADC, DAC, and a precision gain block to perform a set of common tasks. These tasks include: (1) representing an analog signal with one or several digital bits, and (2) generating an error signal, called the residue signal, to be passed to a subsequent stage for further conversion. As a consequence, the most significant bits are generated first, and less significant bits are generated until the residual signal propagates through all stages. Analog-to-digital conversion in a multi-step fashion, as compared to flash ADCs, consumes little power. The increase in power efficiency is a direct result of the reduction in the number of comparators. This can be seen from a comparison between a 10-bit multi-
step ADCs and 10-bit flash ADCs. The 10-bit one-bit per-stage multi-step (pipeline) ADC requires at most 10 comparators (Power \( \equiv 10 \text{ mW} \)). On the contrary, the 10-bit flash ADC requires 1024 comparators (Power \( \equiv 2 \text{ W} \)).

In this chapter, the design and implementation of a 10-bit one-bit per-stage pipeline ADC will be presented. First, a background study on pipeline ADCs will be conducted in Section 4.2. The background study details the underlying principles of operation of pipeline ADCs, as well as various sources of non-idealities. It will be shown that comparator offset is the primary cause of ADC offset error, which could seriously degrade the performance of pipeline ADCs. To reduce the distortion that results from comparator offset, a novel calibration technique will be proposed in Section 4.3. The proposed comparator offset calibration is similar to that introduced in Chapter 2, however adapted for the operation of pipeline ADCs. The proposed calibration method is capable of reducing comparator offset to less than \( 1/2 \text{ LSB} \), while consuming very little power. Detailed design procedures and simulation results will be presented in Section 4.4. Throughout this section, hand analyses and detailed design will be carried out to meet the system level requirements. Finally, in Section 4.5, a systematic top-down design approach will be presented in the design of pipeline ADCs. The top-down approach provides a convenient and quick way of defining system level requirements. It is also capable of facilitating the design of analog circuits by allowing system-level optimization, while maintaining an independence from the underlying silicon process.

4.2 - Background On Multi-step ADCs

A typical multi-step ADC structure is shown in Fig. 4.1, where \( N \) stages are cascaded together. Within each stage, an input signal is first sampled by a T/H circuitry. The sampled input signal is then quantized by the A/D converter to produce the digital output \( B \). Depending on the value of \( B \), an analog residue signal, \( V_{\text{res}} \), is generated and passed to the next stage as input signal for further conversion. The residue signal, \( V_{\text{res}} \), is the amplified quantization error of the A/D conversion. The amplification is defined as \( 2^m \), where \( m \) is an integer.
The structure of a typical multi-step ADC is depicted in Fig. 4.1. Therefore, the operations of multi-step ADCs can be described by a set of common mathematical equations:

Stage 1

\[ B_1 = Quan(V_{in}) \]
\[ V_{res}(1) = 2^{m(1)} \cdot (V_{in} - DAC(B_1)) \] (4.1)

... \[ B_i = Quan(V_{res}(i-1)) \]
\[ V_{res}(i) = 2^{m(i)} \cdot (V_{res}(i-1) - DAC(B_i)) \] (4.2)

Stage n

\[ B_n = Quan(V_{res}(n-1)) \]
\[ V_{res}(n) = 2^{m(n)} \cdot (V_{res}(n-1) - DAC(B_n)) \] (4.3)

where

\[
Quan(v) = \begin{cases} 
    1...11 & \text{if } V_{ref} - \Delta V \leq v \\
    0...01 & \text{if } -V_{ref} \leq v \leq -V_{ref} + \Delta V \\
    0...00 & \text{if } v \leq -V_{ref}
\end{cases}
\] (4.4)

and
where \( +V_{ref} \) and \( -V_{ref} \) are the upper and lower range of the input signal respectively, and \( \Delta V \) is the interval between any two quantization levels.

Among the above equations, variables such as stage resolution (\( B_i \)), stage gain (\( 2^{m(i)} \)), and the number of stages (\( n \)), define the architectural choices for multi-step ADCs. For example, if each stage has a resolution of one bit and a stage gain of two, then a multi-step ADC composed of such a stage is referred to as one-bit per-stage pipeline ADC. Otherwise, it is referred to as a multi-bit pipeline ADC, or multi-bits sub-ranging ADC. Among multi-step ADCs, one-bit per-stage pipeline ADCs are known to be the most power efficient [20]. In this work, effort has been concentrated on designing a low power 10-bit 2-MSPS ADC, while operating under a supply voltage of 1.8 V. Such a requirement mandates a one-bit per-stage pipeline ADC architecture, since it contains the least number of opamps and comparators. Opamps and comparators are the major sources of power consumption. A 10-bit one-bit per-stage pipeline ADC has been designed and implemented in TSMC CMOS 0.18 \( \mu m \) process.

4.2.1 - One-Bit Per-Stage Pipeline ADCs

A simplified single-ended one-bit per-stage pipeline ADC stage is presented in Fig. 4.2. The presented stage accomplishes analog to digital conversion within two non-overlapping clock phases, denoted as \( \phi_1 \) and \( \phi_2 \). For each clock phase, the status of each switch is listed in Table 4.3, and equivalent circuitries are shown in Fig. 4.3. During phase \( \phi_1 \), the opamp is placed in a unity-gain configuration, while driving a load of two capacitors, \( C_1 \) and \( C_2 \) connected in parallel as depicted by Fig. 4.3b. The purpose of placing the opamp into a unity-gain configuration is to sample the input signal, \( V_{in} \), onto
capacitors $C_1$ and $C_2$. Assuming the opamp has an infinite DC gain, bandwidth and slew rate, at the end of $\phi_1$, charges stored in $C_1$ and $C_2$ are, respectively,

\begin{align}
Q_1 &= V_{in} \cdot C_1 \\
Q_2 &= V_{in} \cdot C_2
\end{align}

Due to the sampling action, clock phase $\phi_1$ is commonly referred to as the sampling phase. Immediately after the input signal is sampled, the comparator quantizes the sampled input signal, thus producing a valid output bit, $D$. This bit is then latched and stored in a flip-flop. The stored output bit will be used to determine the output residue signal during the next clock phase, $\phi_2$. During phase $\phi_2$, $C_1$ and $C_2$ are re-arranged such that the top plate of $C_1$ is connected to either $V_{ref}$ or analog ground, depending on the output bit, $D$. The top plate of $C_2$ is connected to the output of the opamp, as depicted in Fig. 4.3c. In the case where $D$ is a logic "low", the top plate of $C_1$ is connected to analog ground, resulting in all the charges stored on $C_1$ being transferred onto $C_2$. At the end of phase $\phi_2$, $C_2$ should contain $(C_1+C_2)\cdot V_{in}$ amount of charge, and $V_{residue}$ is equal to

$$V_{residue} = \frac{(C_1 + C_2)}{C_2} \cdot V_{in}$$

In the case when $D$ is a logic "high", the top plate of $C_1$ is connected to $V_{ref}$ instead. The amount of charge transferred from $C_1$ to $C_2$ is

$$Q_{c_1 \rightarrow c_2} = (V_{in} - V_{ref}) \cdot C_1$$

At the end of phase $\phi_2$, the charge stored in $C_2$ is $C_2V_{in} + (V_{in} - V_{ref}) \cdot C_1$, and the output $V_{residue}$ should be equal to

$$V_{residue} = \frac{C_2 \cdot V_{in} + (V_{in} - V_{ref}) \cdot C_1}{C_2} = V_{in} + C_1 \cdot (V_{in} - V_{ref})$$
Figure 4.2 Typical SC implementation of pipeline ADC

Table 4.3: Timing of various switches

<table>
<thead>
<tr>
<th>Switch/Phase</th>
<th>$\Phi_1$</th>
<th>$\Phi_2$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$S_1$</td>
<td>ON</td>
<td>OFF</td>
</tr>
<tr>
<td>$S_2$</td>
<td>ON</td>
<td>OFF</td>
</tr>
<tr>
<td>$S_3$</td>
<td>OFF</td>
<td>ON</td>
</tr>
<tr>
<td>$S_4$</td>
<td>ON</td>
<td>OFF</td>
</tr>
<tr>
<td>$S_5$</td>
<td>OFF</td>
<td>ON or OFF (Depending on the value of D)</td>
</tr>
<tr>
<td>$S_6$</td>
<td>ON</td>
<td>OFF</td>
</tr>
<tr>
<td>$S_7$</td>
<td>OFF</td>
<td>ON or OFF (Depending on the value of D)</td>
</tr>
</tbody>
</table>
Under an ideal condition where $C_1 = C_2$, the residue voltage, $V_{\text{residue}}$, can be expressed as

\[
\begin{align*}
D = 0 & \quad V_{\text{residue}} = 2 \cdot V_{\text{in}} \\
D = 1 & \quad V_{\text{residue}} = 2 \cdot V_{\text{in}} - V_{\text{ref}}
\end{align*}
\]

The above discussion reveals the basic operating principles behind an one-bit per-stage pipeline ADC. It was assumed that all circuit components such as switches, opamps, capacitors, and comparators are ideal and perfectly matched. Thus, a gain stage of two is achieved, no offset is incurred, and quantization noise is the only error source. However, in practice, switches, opamps, comparators, and capacitors are potential sources of error [22]. In the design of the pipeline ADC, errors can be divided into three categories: noise, gain error, and offset error. The dominant noise is considered to be thermal noise, which originates from the channel of the MOS transistor. Thermal noise is generated, sampled, and amplified in each pipeline stage, degrading the overall signal to noise ratio of the ADCs. It will be shown that thermal noise can be reduced to less than $1/2 \text{ LSB}$ by choosing the appropriate capacitor size ($C_1$ and $C_2$). Gain error refers to any error caused by a deviation from an ideal stage gain of two. The deviation can result from finite opamp gain and bandwidth, slew rate, or capacitor mismatch. Gain error manifests itself as a non-linear distortion, which degrades the THD behavior of the ADC. It will shown that non-
linear distortion induced by a gain error can be minimized to less than 1/2 LSB with careful design choices. Another source of non-linear distortion is the ADC offset error, largely resulting from a non-zero comparator offset. Comparator offset is difficult to minimize, as it depends largely on transistor matching [23]. Fortunately, the offset calibration algorithm proposed in Chapter Two can be adapted to reduce comparator offset, thus improving the overall performance of the ADC. The adaptation of the offset calibration algorithm will be outlined in Section 4.3.

4.2.2 - Thermal Noise

In conventional resistors, thermal noise is due to the random thermal motion of electrons. It is related to absolute temperature $T$ and the value of its resistance $R$. The power spectral density of thermal noise associated with a resistor expressed in units of $V^2/\text{Hz}$ can be written as

$$S(f) = 4kTR$$  \hspace{1cm} (4.12)$$

where $k$ is Boltzmann's constant [23]. The same phenomenon occurs in MOS transistors since the channel region of an MOS transistor has a resistive component. For the applications at hand in this thesis, we shall assume that the channel resistance is $R_{on}$. The pipeline stage shown in Fig. 4.2 contains a number of switches implemented using a NMOS/PMOS pair. Thus, during each clock phase, the corresponding ON-switches act as noise sources, injecting an error charge signal onto capacitors $C_1$ and $C_2$. The amount of noise injected can be calculated by assuming the equivalent circuit model depicted in Fig. 4.4. Here an ideal switch is in series with an on-resistance $R_{on}$ and a voltage noise source. The amount of noise injected is determined by the bandwidth of the equivalent RC network. The total noise power can then be expressed as

$$n^2 = \int_{0}^{\infty} 4kTR_{on} |H_{RC}(j\omega)|^2 d\omega = \int_{0}^{\infty} 4kTR_{on} \left| \frac{1}{1 + j\omega R_{on} C} \right|^2 d\omega = \frac{kT}{C}$$  \hspace{1cm} (4.13)$$

In the design of pipeline ADC, it is imperative to ensure that the input referred noise is below the level of quantization noise. Due to the complexity of the ADC structure, a
detailed noise analysis will be carried out in Section 4.4, where it will be shown how the capacitors can be sized so that the input referred noise meets that desired level.

![Switch Model](image)

Figure 4.4 A typical CMOS switch in a signal path

4.2.3 - Gain Error

In a pipeline stage, gain error refers to the error induced from a stage gain which is either greater or less than the ideal stage gain. In the case where the stage gain is greater than the ideal gain, the resulting residue signal, $V_{residue}$, will exceed $\pm V_{ref}$ the conversion range of the next pipeline stage. The portion of $V_{residue}$ exceeding the conversion range is irreversibly lost, thus resulting in gain error. This type of gain error is also referred to as loss of quantization levels. The other type of gain error occurs when the stage gain is smaller than the ideal gain. In this case, the amplitude of the residue signal, $V_{residue}$, will be smaller than $\pm V_{ref}$, the full conversion range of the next stage. As a direct result, a portion of the residue signal will not be converted. This type of gain error is referred to as loss of quantization codes. Effect of gain error on pipeline ADC's overall transfer characteristics will be demonstrated next, and possible contributing sources will be discussed.

To better understand how gain errors in a pipeline stage affect the converter’s overall transfer characteristic, consider the representation of a 4-bit section of an N-bit pipeline shown in Fig. 4.5. The 3-bit pipeline section in Fig. 4.5a is assumed to be ideal with a resolving range between $+V_{ref}$ and $-V_{ref}$. Fig. 4.5b, Fig. 4.5c, and Fig. 4.5d show the resulting transfer characteristics when the preceding pipeline stage, 1st stage, is also ideal.
and has same resolving range as the 3-bit converter. Referring to Fig. 4.6, the 4-bit pipeline, thus the overall N-bit A/D converter, will have missing codes if the output range of each stage in the pipeline does not completely access the following stage's full input range. For example, Fig. 4.6a shows that if 1st stage is less than 2, D(3) may transition from a logic 0 to logic 1 before the residue signal, $V_{residue}$, reaches within less than 1 LSB of the next section's maximum resolvable input voltage $+V_{ref}$. Loss of quantization codes will result in a vertical discontinuity in the overall DC transfer characteristic curve, which is depicted in Fig. 4.6b. The discontinuity is indicated by a circle. The number of codes lost increases as stage gain creases. The discontinuity is regarded as a source of non-linear distortion.

As discussed before, a stage gain of less than ideal stage gain is the primary cause for the loss of quantization codes. There are multiple sources which could contribute to a small stage gain. Insufficient settling time due to finite opamp bandwidth and slew rate would manifest itself as gain error. In addition, finite opamp gain and capacitor mismatch ($C_1 < C_2$) would also result in a stage gain of less than ideal. An analytical study will be carried out in Section 4.4, where it will be shown how each factor affects stage gain, how each factor can be optimized to meet the desired performance.
Unlike error induced by a smaller stage gain, a stage gain of greater than the ideal stage gain will result in loss of quantization levels. For example, loss of quantization levels will occurs if the difference between the maximum residue of 1st stage and $+V_{ref}$ is larger than 1 LSB. The loss of quantization levels are indicated by circles in Fig. 4.7a. The overall effect due to loss of quantization levels is demonstrated in Fig. 4.7b, where is manifests itself as a horizontal discontinuity. The discontinuity is also regarded as a source of non-linear distortion.

The primary cause behind a large stage gain is due to the mismatch between capacitors $C_1$ and $C_2$ ($C_1 > C_2$). This result can be derived from Eq. (4.8) and Eq. (4.10), where stage gain is defined as $(C_1 + C_2)/(C_2)$. The mismatch between capacitors, with careful layout consideration, can be as small as 0.1% [24][25][25]. It will be shown, in Section 4.4, that error induced by capacitor mismatch is negligible with 0.1% mismatch.
4.2.4 - Offset Error

Offset error refers to the error induced by the existence of comparator offset. Due to the existence of comparator offset, the comparator no longer treats the input signal range as two identical halves, where one half is below comparator threshold, and the other is above the threshold. Thus, with a stage gain of two, loss of quantization levels would occur in the larger input half, while loss of quantization codes occurs in the smaller input half. This is extremely undesirable as it leads to non-linear distortion.

It can be seen that the non-linear distortion will be minimized if the threshold can be shifted back to the ideal position of zero. The most obvious way of minimizing error due
to the offset is to minimize the offset itself. However, this is difficult because comparator offset is sensitive to matching between transistors. Alternatively, one can minimize the effect of the comparator offset by compensating the comparator with a voltage of the same amplitude but of opposite polarity. This can be achieved by the offset calibration algorithm proposed in Chapter Two. In the next section, it will be demonstrated that the offset calibration algorithm can be adapted to the pipeline ADCs, although a slight modification is required.

![Figure 4.8 DC characteristic of pipeline stage due to comparator offset](image)

Figure 4.8 DC characteristic of pipeline stage due to comparator offset

### 4.3 - Digital Calibration for Comparator Offset

Comparator offset minimization presents a similar challenge to that encountered in Chapter Two. To deal with the challenge, a digital DC reference source has been proposed in Chapter Two. It is only logical to adapt the same DC reference source to deal with the comparator offset error in the pipeline ADC. In this section, it will be shown that the digital DC reference source can be exploited to reduce comparator offset error and improve the performance of pipeline ADCs.

- **Calibration Architecture**

For pipeline ADCs, several offset calibration algorithms [26] have been reported. The reported algorithms require either additional opamps or clock cycles to measure, and correct for the offset voltage. These requirements imply either higher power
consumption, or lower conversion speed. In order to design a low-power high-speed pipeline ADCs, it is imperative to advise an alternative calibration algorithm which is capable of minimizing offset in real-time and consumes little power. In this section, a novel offset calibration algorithm will be proposed to satisfy design requirement of low-power high-speed pipeline ADCs.

In order to achieve a 10-bit resolution, the error induced by the comparator offset must not exceed one half of \( \text{LSB} \). To keep the error below \( \frac{1}{2} \text{LSB} \), it has been demonstrated [27] that a comparator offset of less than 0.1% of the input conversion range is required. Such an offset is difficult to achieve across all process corners [29], however, it is only essential to the pipeline stages which generate the most significant bits (MSBs). The MSBs’ stages are calibrated because they are required to be as linear as the entire pipeline ADC [20][21][25]. The proposed offset calibration, consisting of two independent digital DC reference sources, is depicted in Fig. 4.9. The DC reference sources are designed to measure the comparator offset of each stage. The measured offset are encoded in \textit{Bitstream 1} and \textit{Bitstream 2}, which is then used to correct for the offset during the normal operation of pipeline ADCs.

The calibration process is similar to that introduced in Chapter Two. The detailed implementation of the proposed calibration algorithm will be discussed next.

![Diagram of novel comparator offset calibrated pipeline ADC architecture.](image)

\[ R_1 = R_2 = 280 \, \text{K}\Omega \]
\[ C_1 = C_2 = 27 \, \text{fF} \]

\( \text{Figure 4.9} \) Novel comparator offset calibrated pipeline ADC architecture.
• Design Strategy

The digital DC reference source, presented in Chapter Two, is capable of generating a stable and accurate DC voltage. The DC reference source consists of a flip-flop chain and a RC low pass filter as shown Fig. 4.10. During the offset calibration process, the flip-flop chain is loaded with a ΣΔ bitstream which is generated with software in real time. The ΣΔ bitstream encodes a desired DC reference whose resolution is determined by the length of the flip-flop chain. For example, a flip-flop chain with length of 1024 is capable of producing a DC voltage with a ripple less or equal \( V_{\text{range}}/1024 \).

![1024 flip-flops](image)

**Figure 4.10** Memory based digital DC level generator

In each pipeline stage, the output of the DC generator \( V_{dc} \) is connected to the negative terminal of the comparator, while either \( V_{in} \) or \( V_{ref} \) is connected to the positive terminal depending on the mode of operation. This is shown in the basic calibration topology of Fig. 4.11, where the comparator is modeled as an ideal comparator with an offset voltage, \( V_{\text{offset}} \). To generate a DC reference, the flip-flop chain is loaded with either a pulse density modulated (PDM) or a pulse width modulated (PWM) bitstream. The PDM or PWM bitstream encodes the DC reference. The DC tone is then extracted from the bitstream by passing it through the RC filter. The PDM or PWM bitstream can be easily derived either from an on-chip source (a digital ΣΔ modulator or a digital counter) or by downloading an appropriate bitstream generated in software. Experiments conducted so far have shown that the digital DC reference generator is relatively process and temperature invariant (<200 ppm/°C).
The offset calibration process takes place only once during the start-up phase and lasts for roughly 100 ms. The calibration process is divided into two phases: (a) offset measurement and (b) offset correction. In the offset measurement phase, the flip-flop chain is loaded with a digital bitstream which encodes a DC reference level. This bitstream is cycled around within the flip-flop chain and its encoded DC reference is extracted by the low-pass filter. The extracted DC reference is compared with $V_{\text{ref}}$ by the comparator, as indicated in Fig. 4.12b. Initially, a bitstream, $B(0)$, representing $V_{dc}$ is loaded into the flip-flop chain which makes the comparator produce a logic one, i.e. $V_{dc} < V_{\text{ref}} - |V_{\text{offset}}|$. The value of $V_{dc}$ is then incremented by one LSB (one LSB = $V_{\text{supply}}/2^M$). This is achieved by loading a new encoded bitstream into the flip-flop chain that represents the incremented DC value. The process is repeated until a change in logic level occurs at the output of the comparator as shown in Fig. 4.12c. The bitstream that caused the transition, $B(m)$, is saved into memory. The saved bitstream contains two components: $V_{\text{ref}}$ and $-V_{\text{offset}}$. In the offset correction phase shown in Fig. 4.12d, the saved bitstream is loaded into the flip-flop chain, and the output of the RC low-pass filter is connected to the negative terminal of the comparator. The offset that is present on the input signal, which is connected to the positive terminal of the comparator, is cancelled by the presence of
-\(V_{offset}\) in the extracted DC reference. Through the calibration process, comparator offset are reduced to exactly one \(LSB\).
Monolithic Nyquist Rate ADC With Digital Calibration  

With Digital Calibration Multi-Step ADCs

![Diagram of Monolithic Nyquist Rate ADC with Digital Calibration]

**Figure 4.12 Comparator offset calibration process**

---

**a) Basic topology**

---

**b) Close switch \( S_1 \) and load DC generator with bitstream \( B(0) \)**

---

**c) Different DC bitstream are loaded until \( Q \) change from 0 to 1. Save the bitstream \( B(m) \) which caused transition**

---

**d) Open switch \( S_1 \) and close switch \( S_2 \). The comparator is fully calibrated**

---

**Figure 4.12 Comparator offset calibration process**
To demonstrate the effectiveness of the offset calibration algorithm, Hspice simulations have been performed with and without the algorithm. It is assumed that a low frequency signal \((f_{in} = 146.5 \text{ KHz})\) is the input to ADC. Without offset calibration, the comparator offset has a standard deviation, \(\sigma = 30 \text{ mV}\). With offset calibration, comparator offset is limited to 1 \(\text{ LSB}\) \((1.0 \text{ V} / 1024 = 0.977 \text{ mV})\). SNDR plot for both cases are shown in Fig. 4.13. As it is shown, without offset calibration, non-linear distortion manifest itself as a number of harmonics in Fig. 4.13a, and only 40 dB SNDR is achieved. However, after offset calibration, the harmonics are removed since there is no offset induced missing codes or levels. With offset calibration, 61.8 dB SNDR is achieved.

![SNDR Plot Without Offset Calibration](image1)

**a) SNDR plot without offset calibration, SNDR = 40 dB**

![SNDR Plot With Offset Calibration](image2)

**b) SNDR plot with offset calibration, SNDR = 61.8 dB**

*Figure 4.13 SNDR plot with and without offset calibration algorithm*
4.4 - Design and Implementation Issues

In the background study in Section 4.2, it has been shown that thermal noise, gain error, and offset error are some of the most significant errors in pipeline ADCs. These errors either degrade signal to noise ratio, or induce non-linear distortion. Non-linear distortion induced by the offset error is correctable through the use of the offset calibration algorithm proposed in Section 4.3. However, the reduction of thermal noise and gain error requires further study. In this section, the contributing sources to thermal noise and gain error, such as switches, capacitors matching, and opamp, will be explored in detail. Design strategies will be proposed to minimize the effect of error sources.

4.4.1 - Switch Related Problems

In switched-capacitor (SC) circuits, the switch is one of the most critical components. Without careful design consideration, it can be one of the most significant sources of error. For example, the switch generates considerable thermal noise, thus degrading the signal to noise ratio. Charge injection, induced by the release of charges stored in the channels of the transistors of the switches, will modify the pipeline stage gain, thus leads to potential non-linear distortion. In addition, large and non-linear switch on-resistance could limit the bandwidth of pipeline ADCs. In this subsection, these switch related problems will be addressed in detail, and remedies will be proposed.

1. Switch Thermal Noise ($kT/C$ noise)

Pipeline stage, shown in Fig. 4.2, is implemented with switched-capacitor technology. The stage contains seven switches. Each switch can be modeled as a thermal noise source in series with on-resistance $R_{on}$ and an ideal switch as depicted in Fig. 4.4. During the sampling phase and evaluation phase, thermal noise is sampled along with the input signal, and amplified. The amplified signal is then passed to the next stage. For 10-bit pipeline ADCs, the sampling and amplification of switch thermal noise occurs at each stage. Thus, it is imperative to understand how the thermal noise interacts within pipeline ADCs, and how the thermal noise can be controlled to an acceptable level ($< 1/2 LSB$).
To simplify the study of the effect of thermal noise on the overall pipeline ADC, the switch thermal noise of the different switches are assumed to be statistically independent. With the simplification, a pipeline ADC noise model can be established, which is demonstrated in Fig. 4.14. In each stage, it is assumed that, during the sampling phase, the thermal noise sampled onto capacitors \((C_1 \text{ and } C_2 \text{ shown in Fig. 4.2})\) is dominant. This is valid since the sampled thermal noise sets an upper limit for the overall signal to noise ratio. Thus, only one thermal noise source, \(n_{KT/C}\), is modeled for each stage. During normal operation of pipeline ADCs, the thermal noise is summed with input the signal, and amplified reliably, and passed onto the next stage.

From the model introduced in Fig. 4.14, the total input referred thermal noise can be calculated as

\[
V_N^2 = \frac{KT}{C} + \frac{KT}{C} \cdot \frac{1}{4} + \ldots + \frac{KT}{C} \cdot \frac{1}{n^2}
\]  

(4.14)

where each stage has identical value of capacitance \((C = C_1 + C_2)\) [24][28]. As indicated by Eq. (4.14), if the capacitance, \(C\), is sufficiently large, the resulting total thermal noise, \(V_N^2\), can be reduced to below the quantization noise. This implies that, in order to obtain the desired \(SNR\), the following must be valid:

\[
\frac{KT}{C} + \frac{KT}{C} \cdot \frac{1}{4} + \ldots + \frac{KT}{C} \cdot \frac{1}{n^2} < \frac{(\Delta/2)^2}{12}
\]  

(4.15)
where $\Delta = 1$ LSB of ADC. Assuming $n$ is large ($n + 10$) enough, an lower bound for stage capacitance can be obtained by further reducing Eq. (4.15). The lower bound of stage capacitance is given as

$$\frac{KT}{C} \left(1 + \frac{1}{2^2} + \ldots + \frac{1}{n^2}\right) < \frac{(\Delta/2)^2}{12}$$

$$\frac{KT}{C} \cdot 2 < \frac{\Delta^2}{48}$$

$$C > \frac{KT \cdot 96}{\Delta^2}$$  

(4.16)

From Eq. (4.16), one can easily find out the minimum stage capacitance by substituting $\Delta$ with an appropriate value. For example, for a 12-bit pipeline ADC with $1 V_{pp}$ input range, $\Delta$ is 0.244 mV and a capacitor of 7 pF is sufficient to ensure that the thermal noise is well below 75 dB. A Hspice noise simulation on 12-bit pipeline ADCs is present in Fig. 4.15, where a plot of achievable SNR versus a large range of capacitor size is demonstrated. The figure confirms that the pipeline ADC will achieve a 12-bit resolution if capacitor size is greater than or equal to 7.0 pF.

It is interesting to note that, in Eq. (4.14), the later stages contribute negligible amount of thermal noise. For example, the last stage contributes $1/n^2$ of $kT/C$ noise, given all stages have the same capacitance value. This could be advantageous in designing a low power
pipeline ADC. In designing a low power pipeline ADC, smaller capacitors are preferred since, in switched-capacitor circuits, part of power is dissipated through the process of charging and discharging capacitors. According to Eq. (4.14), different stage contributes different amount of the input referred thermal noise. Therefore, each stage can be optimized to provide minimum power consumption and still inject acceptable thermal noise. This can be done by choosing the nominal size capacitors in the first stages, while adopting smaller capacitors in the later stages. This technique provides a good balance between power consumption and thermal noise; however, the stages will differ from each other and have to be laid out individually.

2. Switch Charge Injection
During the operation of switched capacitor circuits, switches are frequently turned on and off. During on time, the switch acts as a capacitor, storing charge within the channel of transistors. And when transistors are turned off, the stored charges are released due to the disappearance of the channel. Part of the released charges will end up in the sampling capacitor \((C_1 \text{ and } C_2)\), thus disturbing the sampled voltage in the capacitor. In the case of the pipeline ADC, the disturbance of the sampled voltage will result in a modified stage gain, thus leading to potential non-linear distortion. In this section, charge injection, will be studied in detail.

*CMOS Switch*

To ensure a large input dynamic range, a complementary MOS switch is preferred for it is capable of conducting an input signal that is closer to either supply rail. For example, in a simplified track and hold circuit shown in Fig. 4.16a, the PMOS is ON and the NMOS is OFF when the input signal is close to the upper rail, and vice versa. When the input signal is close to the mid-rail, both NMOS and PMOS is ON. Depending on the state of the MOS transistors, the operation of the switch can be categorized into three regions. Among these three operating regions depicted in Fig. 4.17, charge injection is minimum in region II. This is due to the cancellation of opposite charges injected by NMOS and PMOS after they are both turned off. However, in either region I or III, only one of the MOS transistors is turned on and operates in the triode mode. When the on-switch is turned off, there is no
cancellation of opposite charges from the off-transistor. Thus, charge injection is more severe.

![CMOS switch and small signal MOS transistor parasitic](image)

Figure 4.16 CMOS switch and small signal MOS transistor parasitic

Figure 4.17 Relation between input signal amplitude and charge injection

It is difficult to quantify the amount of charge injected into the sampling capacitor. A worst case analysis will be discussed here. In the worst case, it is assumed that all the charge stored in the MOS transistor is injected into the sampling capacitor. Before carrying out the analysis, a general assumption is made such that the input signal $V_{\text{in}}$ has a amplitude of $V_A$ and is centered around the mid-rail, and the supply voltage is $V_{dd}$. The variation in the charge injected can be expressed as

$$\Delta Q = \left[ \frac{V_{dd}}{2} + \frac{V_A}{2} \right] \cdot \left( C_{Ng1ot} + C_{Pg1ot} - C_{Ngd} - C_{Pgda} \right)$$  

(4.17)
where $C_{gtotal}$ is the total NMOS gate capacitance, $C_{ptotal}$ is the total PMOS gate capacitance, $C_{gd}$ is the total NMOS gate to drain capacitance, and $C_{pgd}$ is the total PMOS gate to drain capacitance [29]. The value of the various capacitance can be obtained from the CMOS model provided by Fibs (0.18 $\mu$m from TSMC). For a sampling capacitor of size $C_s$, the charge injection induced error in voltage is given as

$$\Delta V = \Delta Q \cdot C_s \quad (4.18)$$

Hspice model also seems to adopt a worst case analysis. A hand analysis result of the worst case is compared against the Hspice simulation for a set of switches with different sizes in Table 4.4.

<table>
<thead>
<tr>
<th>Transistors' Size (um)</th>
<th>Hand Analysis</th>
<th>Hspice Simulation</th>
<th>% error</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>$V_{in}=1.627$</td>
<td>$V_{in}=0.172$</td>
<td></td>
</tr>
<tr>
<td>NMOS: W/L=10/2</td>
<td>0.083 V</td>
<td>-0.076 V</td>
<td>1.9 %</td>
</tr>
<tr>
<td>PMOS: W/L=10/2</td>
<td>0.167 V</td>
<td>-0.151 V</td>
<td>3.9 %</td>
</tr>
<tr>
<td>NMOS: W/L=20/2</td>
<td>0.334 V</td>
<td>-0.304 V</td>
<td>17.8 %</td>
</tr>
<tr>
<td>PMOS: W/L=20/2</td>
<td>0.299 V</td>
<td>-0.245 V</td>
<td></td>
</tr>
<tr>
<td>NMOS: W/L=40/2</td>
<td>0.299 V</td>
<td>-0.245 V</td>
<td></td>
</tr>
<tr>
<td>PMOS: W/L=40/2</td>
<td>0.299 V</td>
<td>-0.245 V</td>
<td></td>
</tr>
</tbody>
</table>

As shown in Table 4.6, the hand analysis is closely matched by Hspice simulation. The hand analysis can be helpful in estimating the amount of charge injection errors in future studies. To remedy the charge injection problem, the addition of dummy switches has been widely adopted. In this work, dummy switch has also been used to minimize the amount of charge injected into the sampling capacitors.

**Dummy Switch**

Dummy switch has been proposed, and widely used to minimize the charge injection problem [30]. A dummy switch is shown in Fig. 4.18. The dummy switch is designed to be half of size of the switch which is proceeding it. It is assumed that, when the switch is turned off, the charge stored in the channel is split evenly between drain and source. Therefore, $1/2 \Delta Q$ is moved toward the sampling capacitors. The dummy switch, located
between the switch and the sampling capacitor, absorbs exactly the 1/2 ΔQ charge. Thus, the sampling capacitor experiences no additional charge.

![Figure 4.18 Absorption of charge injection by dummy switch](image)

In Table 4.5, Hspice simulation has been conducted to study the performance difference between addition of dummy switch, and absence of dummy switch. The simulation is conducted with a sampling frequency of 10.24 MHz, and an input sinusoidal signal with an amplitude of 0.9 V and a frequency of 310 KHz. An 1 pF capacitor is used as the hold capacitor. It can be shown there is a definite improvement as the dummy switch is added. The presence of the dummy switch is essential in design of low-distortion circuitries.

<table>
<thead>
<tr>
<th>Transistors' Size (um)</th>
<th>With dummy switch (dB)</th>
<th>Without dummy switch (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>NMOS: W/L=10/2 PMOS: W/L=10/2</td>
<td>46.7</td>
<td>41.1</td>
</tr>
<tr>
<td>NMOS: W/L=20/2 PMOS: W/L=20/2</td>
<td>51.8</td>
<td>37.0</td>
</tr>
<tr>
<td>NMOS: W/L=40/2 PMOS: W/L=40/2</td>
<td>54.6</td>
<td>27.8</td>
</tr>
</tbody>
</table>

3. Switch Nonlinear On-Resistance

In a SC implementation of pipeline ADCs, variation in switch on-resistance could also affect performance of pipeline ADCs. To study the effect of switch on-resistance, a switch model is demonstrated in Fig. 4.19, where switch is modeled as an ideal switch in
series with channel resistance $R_{on}$. The resistance, $R_{on}$, is input voltage, $V_{in}$, dependent. In this section, the first-order effect of switch on-resistance will be presented.

In a first-order approximation, switch on-resistance, $R_{on}$, can be modeled as two resistors in series. One of the resistors is defined as nominal resistance, $R_{nominal}$, which is the average switch on-resistance over a pre-defined input voltage range. The other resistor, $R_{V_{in}}$, is the variable resistance. The overall model of on-resistance is expressed as

$$R_{on}(V_{in}) = R_{nominal} + R_{V_{in}}$$

(4.19)

where $R$ ($\Omega$/V) is slope of the first-order approximation model as shown in Fig. 4.19.

Assuming initially that $V_o = 0$, and in the worst case, $V_{in}$ varies from 0 to $V_{dd}$ (Input signal slew rate $= V_{dd}/T$, where $T$ is the switch on-time), the following two equations are valid:

$$i = C \frac{dV_o}{dt}$$

(4.20)

$$i = \frac{V_{in} - V_o}{R_{on}(V_o)}$$

(4.21)

By re-arranging Eq. (4.20) and Eq. (4.21), it can be shown that

$$C \frac{dV_o}{dt} + \frac{1}{R_{nominal} + R \cdot \frac{V_{dd}}{T} \cdot t} \cdot V_o = \frac{(V_{dd}/T) \cdot t}{R_{nominal} + R \cdot \frac{V_{dd}}{T} \cdot t}$$

(4.22)

By evaluating Eq. (4.22) at time $t = T$, it can be shown that

$$V_o(T) = \frac{V_{dd}}{R_{nominal} C + R \cdot \frac{V_{dd}}{T} \cdot C \frac{1}{T} + 1}$$

(4.23)

Eq. (4.23) can be useful in estimating the maximum allowed variation in channel resistance in order to achieve the desired resolution. For example, in order to achieve 10-bit resolution, the error induced by the variation in switch on-resistance should not exceed $1/2$ LSB of ADC

$$\Delta error = V_{dd} - V_o(T) \leq \frac{1}{2} \cdot LSB$$

(4.24)
Alternatively, it means that, for a given $T$, as long as the sum of $R_{\text{nominal}}C$ and $RV_{dd}C$ is less than 0.1% of switch on-time, $T$, the induced error will be well below that of quantization noise.

![Switch model](image_a)

![Switch on-resistance model](image_b)

Figure 4.19 Switch model and switch on-resistance model

### 4.4.2 - Capacitor Mismatch

As discussed in Section 4.2, matching between capacitors is one of the determining factors of pipeline stage gain. As shown in Fig. 4.3a, during phase $\phi_1$, the input signal, $V_{in}$, is sampled into both $C_1$ and $C_2$. $C_1$ and $C_2$ contain charge $Q_1$ and $Q_2$ respectively, where

\[ Q_1(\phi_1) = V_{in} \cdot C_1 \]  
\[ Q_2(\phi_2) = V_{in} \cdot C_2 \]

And during phase $\phi_2$, the evaluation phase, the charge stored in $C_1$ is forced into capacitor $C_2$, causing the opamp output to rise to

\[ V_{out} = \frac{Q_2(\phi_2)}{C_2} \]

\[ = \frac{(C_1 + C_2) \cdot V_{in}}{C_2} \]

As indicated in Eq. (4.27), the stage gain depends on the ratio of $C_1$ and $C_2$. Under an ideal situation where $C_1 = C_2$, the ideal stage gain is exactly 2. However, due to
limitation of IC fabrication technology, matching is typically limited to 0.1%, which gives an upper bound on the performance of pipeline ADC. The upper bound is commonly considered to be at most 12 Bits.

Using Hspice simulation, a plot of performance (SNDR) vs. capacitors matching has been obtained. The plot is demonstrated in Fig. 4.20, where a 0.1% mismatch in capacitance results in a SNDR of 70 dB, which is equivalent to 12-bit resolution. For a 10-bit pipeline ADC, capacitance mismatch of up to 0.5% can still be tolerated. Thus, in the design of 10-bit pipeline ADC, no capacitor mismatch cancellation techniques are required. Closely coupled capacitors \( C_1 \) and \( C_2 \) laid out in a centroid fashion should guarantee the required matching requirement.

![Figure 4.20 Achievable SNDR vs. capacitor mismatch.](image)

4.4.3 - Opamp Design

The Opamp is another crucial component in the design of pipeline ADCs. Opamp parameters such as DC gain, bandwidth, and slew rate are the three most important factors which limit the precision and speed of the pipeline ADC. In the following three subsections, it will be shown how the opamp can be designed to meet the performance requirement for a 10-bit pipeline ADC.
1. Opamp DC Gain

![Diagram of pipeline stage two phase operation]

Figure 4.21 Pipeline stage two phase operation.

The gain of the opamp is directly related to the stage gain of a pipeline ADC. In Fig. 4.21, it is assumed that $C_1 = C_2$, and opamp is assumed to have a gain of $A$. During $\phi_1$, $V_{in}$ is sampled onto both $C_1$ and $C_2$. The charge stored in $C_1$ and $C_2$ are, respectively,

$$Q_1(\phi_1) = C_1 \cdot V_{in}$$  \hspace{1cm} (4.28)

$$Q_2(\phi_1) = C_2 \cdot V_{in}$$  \hspace{1cm} (4.29)

During $\phi_2$, some charge stored in $C_1$ is transferred into $C_2$. The amount of charge which is left in $C_1$ is

$$Q_1(\phi_2) = C_1 \cdot V_d$$  \hspace{1cm} (4.30)

where

$$V_d = \frac{V_{out}}{A}$$  \hspace{1cm} (4.31)

Therefore, total amount of charge which is stored in $C_2$ can be found as

$$Q_2(\phi_2) = Q_2(\phi_1) + Q_1(\phi_1) - Q_1(\phi_2)$$

$$= C_2 \cdot V_{in} + C_1 \cdot V_{in} - \left( C_1 \cdot \frac{V_{out}}{A} \right)$$  \hspace{1cm} (4.32)
which can be simplified further to determine $V_{out}$ as

$$V_{out} = \frac{Q_2(\phi_2)}{C_2} + V_d$$

$$= \left[ (C_1 + C_2) \cdot V_{in} - \left( \frac{C_1}{A} \cdot V_{out} \right) \right] / C_2 + \frac{V_{out}}{A}$$

(4.33)

$$A = \frac{V_{out}}{V_{in}} = \left( \frac{C_1 + C_2}{C_2} \right) \left( \frac{1}{A} + 1 \right) \cdot V_{in}$$

(4.34)

In Eq. (4.34), if $A$ is infinite, the denominator approaches 1. Thus, stage gain, defined as $V_{out}/V_{in}$, is reduced to 2. However, the DC gain of an opamp is typically limited to 60dB - 80dB over a finite range of bandwidth. The finite DC gain degrades the performance of the pipeline ADC through the loss of quantization code. The loss of quantization code has been explained in details in Section 4.2.

In a typical design, the error induced by loss of codes should be minimized to less than 1/2 LSB of ADCs. The loss of codes induced errors can be calculated as

$$\Delta error = (V_{out} - \bar{V}_{out}) < \frac{1}{2} \cdot LSB$$

(4.35)

where $V_{out}$ is ideal output with a stage gain of 2, and $\bar{V}_{out}$ is non-ideal output with stage a gain less than 2. To achieve the required error level, the opamp DC gain should be at least

$$\Delta error = V_{out} - \bar{V}_{out}$$

$$= (2 - A) \cdot V_{in} < \frac{1}{2} \cdot LSB$$

(4.36)

which means

$$2 - 2 \left( 1 + \frac{1}{A} \right) < \frac{1}{2} \cdot LSB$$

$$A > 4 \cdot \frac{1}{LSB}$$

(4.37)
The opamp DC gain, $A$, should be at least $4/\text{LSB}$ in order to ensure that no code is missing. For example, for a 10-bit pipeline ADC, opamp DC gain, $A$, has to be at least

$$A = 4 \cdot \frac{1}{\text{LSB}}$$

$$= 4 \cdot \frac{1}{2^{-9}}$$

$$= 2048 \quad \text{V/V}$$

(4.38)

, or equivalently 66 dB. Hspice simulation, shown in Fig. 4.22, demonstrates that with the DC opamp obtained in Eq. (4.38), $A = 2048 \quad \text{V/V}$, a SNDR of 59 dB can be achieved, which is close to theoretical limit for a 10-bit ADC.

![SNDR vs. Opamp DC Gain](image)

Figure 4.22 Achievable SNDR vs. opamp DC gain.
2. Opamp Bandwidth

In this section, the bandwidth requirement will be investigated and presented in a quantitative way. Careful selection of opamp bandwidth is crucial, since it will affect bandwidth, distortion, and noise level in pipeline ADCs.

![Opamp Symbol and Frequency Response](image)

In Fig. 4.21, it is assumed that \( \phi_1 = \phi_2 = 1/(2F_s) \), where \( F_s \) is the sampling rate of pipeline ADCs. During \( \phi_1 \), the opamp is in the unity-gain configuration. And during \( \phi_2 \), the opamp is connected in the feedback configuration with nominal gain of 2. One way to study the effect of the bandwidth on the performance of the pipeline ADC is to investigate the worst case scenario which occurs only in \( \phi_2 \), the evaluation phase. The phase \( \phi_2 \) is the worst scenario because, during this phase, the opamp is in the highest feedback gain configuration, thus has the lowest bandwidth.

Assuming an input signal \( V_{in} \) is applied as shown in Fig. 4.21 and no slewing occurs, the opamp in the feedback configuration can be modeled as a RC network with a time constant \( \tau \). In order to induce no missing codes, the time constant \( \tau \) must satisfy

\[
\Delta error = V_{ideal-out} - V_{out} < \frac{1}{2} \cdot LSB
\]

(4.39)
where $V_{\text{ideal-out}}$ is the ideal output voltage, $2 \cdot V_{in}$, and

$$V_{out} = 2 \cdot V_{in} \cdot \left(1 - e^{-\frac{T_s/2}{\tau}}\right)$$  \hspace{1cm} (4.40)

From Eq. (4.40), one can derive the worst case time constant $\tau$, which is expressed as

$$\tau \leq \frac{T_s/2}{\ln\left(\frac{4}{\text{LSB}}\right)}$$  \hspace{1cm} (4.41)

In frequency domain, the 3dB frequency of the system with gain of 2

$$f_{3dB} = \frac{1}{2\pi \cdot \tau} \geq \frac{1}{2\pi} \cdot \frac{\ln 4 - \ln(\text{LSB})}{T_s/2}$$  \hspace{1cm} (4.42)

Assuming that the product of bandwidth and gain is a constant, the minimum unity gain bandwidth can be expressed as

$$f_{UGBW} = 2 \cdot f_{3dB} = \frac{2}{2\pi} \cdot \frac{\ln 4 - \ln(\text{LSB})}{T_s/2} = \frac{2}{\pi} \cdot \frac{\ln 4 - \ln(\text{LSB})}{T_s}$$  \hspace{1cm} (4.43)

For example, for a 10-bit pipeline ADC with a sampling rate of 10 MHz, the pipeline stage opamp must have an unity-gain bandwidth of 53 MHz

$$f_{UGBW} = \frac{2}{\pi} \cdot \frac{\ln 4 - \ln(2^{-10})}{10^{-7}} \approx 55 \text{ MHz}$$  \hspace{1cm} (4.44)

The $f_{UGBW}$ is a very minimum requirement for designing a 10-bit pipeline ADC with a sampling rate of 10 MHz. It is the minimum requirement because the opamp is assumed to not to have slewed. This assumption is only valid if the opamp is designed to have a large slew rate, which will be addressed next.

3. Opamp Slew Rate

The previous analysis is based on one important assumption: the opamp doesn’t slew. In reality, opamp has limited slew rate, thus it could slew if not properly designed or subjected to power constraints. Assuming the opamp has infinite gain, time constant $\tau$, 

\hspace{1cm}
and slew rate $SR$, opamp is configured in unity gain configuration. At time $t$, the opamp output can be expressed as [31]

$$V(t) = SR \cdot \lambda + (V_{\text{ideal-out}} - SR \cdot \lambda) \cdot (1 - e^{-t/\tau})$$

(4.45)

where $V_{\text{ideal-out}}$ is the ideal value which the opamp should settle to, and $\lambda$ is the transition point where the opamp leaves the slew limited region and enters the bandwidth limited region. $\lambda$ can be calculated as

$$\lambda = \frac{V_{\text{ideal-out}}}{SR} \cdot \tau$$

(4.46)

The minimum slew rate required to achieve a given resolution at a given speed can be calculated using same method as shown in previous subsections. Typically, to ensure that no code is missing, the error, defined as $V_{\text{ideal-out}} - V(T_s/2)$, must be smaller than $1/2$ LSB. This requirements is formulated in Eqn. (4.47),

$$\Delta \text{error} = V_{\text{ideal-out}} - V\left(\frac{T_s}{2}\right) \leq \frac{\text{LSB}}{2}$$

(4.47)

where $T_s/2$ is amount of time in which opamp settles.

In the worst case, for an opamp with a 3dB bandwidth at $f_{3\text{dB}}$, opamp slews during the entire time $(T_s/2)$. The error induced by slewing must be less than $1/2$ LSB. In order to meet the error requirement, a minimum slew rate, $SR$, is indicated by Eq. (4.48)

$$SR \geq \frac{V_{\text{ideal-out}}}{\lambda} - \left(\frac{\text{LSB} \cdot T_s}{2 \cdot \lambda \cdot e^{-T_s/2/\tau}}\right)$$

(4.48)

is required. For 10-bit pipeline ADC with 10 MHz sampling clock and input signal range of $1.0 \, V_{\text{pp}}$ $(V_{\text{ideal-out}} < 1.0 \, V)$, a minimum slew rate of $30 \, \text{V/\mu s}$ is required.

4. Opamp Implementation Details

The requirement for DC gain, bandwidth, and slew rate has been demonstrated in the hand analyses carried out in previous subsections. In order to design a 10-bit 10-MSample/s
pipeline ADC in the TSMC 0.18 μm CMOS process, it can be shown that the following specifications for the opamp are required:

Table 4.6: Opamp specification (10 pF load)

<table>
<thead>
<tr>
<th>Specification (Determined by Simulation)</th>
<th>Actual Design (Hspice Simulation)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage (V)</td>
<td>1.8</td>
</tr>
<tr>
<td>DC Gain (dB)</td>
<td>72.0</td>
</tr>
<tr>
<td>UGBW (MHz)</td>
<td>53 MHz</td>
</tr>
<tr>
<td>Phase Margin (Degree)</td>
<td>45.0</td>
</tr>
<tr>
<td>Slew Rate (V/μs)</td>
<td>30.0</td>
</tr>
<tr>
<td>Power (mW)</td>
<td>N/A</td>
</tr>
</tbody>
</table>

An opamp with folded cascode architecture has been chosen for this implementation. The opamp topology is shown in Fig. 4.24. The folded cascode architecture is suitable for very low supply voltage (\( V_{\text{supply-min}} = |V_T| + 2 |V_{\text{DS,min}}| \)), and offers a larger output swing as compared to other architectures (i.e. Two stage Class A, or Two stage Class A/AB). In addition, a low power consumption of 2.03 mW has been achieved with this architecture.

In designing the folded cascode opamp, the opamp has a gain determined by the \( g_m \) of differential transistor pairs M1 and M2 (W=12μm, L=1μm, Multiplier=4). The differential pairs are biased such that \( I_{D1} = I_{D2} = 50 \mu A \) when balanced. The opamp gain, \( A_v \), can be expressed as

\[
A_v = g_m r_{\text{out}}
\]  

(4.49)

where \( r_{\text{out}} \) is the output impedance "looking" into the output terminals (\( V_{\text{out+}} \) or \( V_{\text{out-}} \)).

The unity gain bandwidth (UGBW) can be expressed as a product of DC gain and 3dB frequency,

\[
UGBW = A_v \cdot f_p
\]  

(4.50)

where the dominant pole is located at

93
By combining Eq. (4.50) and Eq. (4.51), UGBW can be expressed in term of \( g_m \) and load capacitor \( C_{out} \):

\[
UGBW = \frac{g_m}{2\pi \cdot C_{out}}
\]  

(4.52)

The output impedance of the opamp, \( r_{out} \), is determined as

\[
r_{out} = r_{outPMOS} \parallel r_{outNMOS}
\]  

(4.53)

where

\[
r_{outPMOS} = g_m r_{rd7} r_{ds9}
\]  

(4.54)

and

\[
r_{outNMOS} = g_m r_{ds5} (r_{ds3} \parallel r_{ds1})
\]  

(4.55)

The complete folded cascode opamp, shown in Fig. 4.24, contains a CMFB which is set to be 0.825 V. Both \( I_{bias1} \) and \( I_{bias2} \) are set to be 150 \( \mu \)A each. DC analysis, transient analysis, frequency analysis have been performed in Hspice simulation, and the results are shown in Fig. 4.25 and Fig. 4.26. The simulation meets the requirement as defined that of Table 4.6.
Monolithic Nyquist Rate ADC With Digital Calibration

Multi-Step ADCs

Figure 4.24 Differential opamp with common-mode feedback.

Figure 4.25 Opamp DC and transient analysis
Comparator Design

The comparator is one of the most crucial components in any analog to digital convertor design. For the pipeline ADC, comparator is desired to possess low offset, while consuming little power and area. Traditionally, to reduce the comparator offset, several methods have been employed. One of them is to use a pre-amp stage which then drives a latched-comparator. The pre-amp circuitry not only adds power, but also increases the size of the comparator. Other methods include employing auto-zeroing circuitry, or using large size transistors in order to reduce mismatch [32]. All these methods contribute either more power, or larger area, or both. In this chapter, reduction of the comparator’s offset has been achieved with the digital reference source introduced before. Thus, for the comparator design, it is desired to have a simple and low-powered latched comparator which meets the basic settling requirement. The settling requirement demands that the comparator must settles within $1/(2F_s) = 50 \text{ ns}$, where $F_s$ (10 MHz) is the sampling rate.

In the design of a 10-Bit pipeline ADC, a latched comparator [22][33] has been chosen for its simplicity and low-power consumption. The latched comparator, shown in Fig. 4.27a, doesn’t require any biasing current network; therefore, consumes no static power. The latched comparator is required to resolve a voltage equivalent of to $1/2 \text{ LSB} \sim 0.5 \text{ mV}$ within 50ns. This can be accomplished by sizing the transistors carefully. The dimension
of all transistors are listed in Fig. 4.27, and a Hspice simulation of comparator, shown in Fig. 4.28a and Fig. 4.28b, confirms that the latched comparator is capable of resolving at least 1.0 mV well within 50 ns.

\[
\begin{align*}
M1 = M2 = M4 = M5 : W &= 10 \mu\text{m}, L = 3.5 \mu\text{m}, M = 2 \\
M6 = M7 = M8 = M9 : W &= 10 \mu\text{m}, L = 2.0 \mu\text{m}, M = 4 \\
M_{\text{CLK}} : W &= 20 \mu\text{m}, L = 2.0 \mu\text{m}, M = 4
\end{align*}
\]

Figure 4.27 Latched comparator

Figure 4.28 Hspice simulation of the latched comparator
4.5 - Parameter Selection Strategy: A Top-Down Design Approach

During traditional analog design process, it is not uncommon for people to ask various questions about system-levels requirements before proceeding to circuit level design. The questions could range from “how fast does the opamp have to be?”, “what DC gain should the opamp possess?”, to “what degree of matching between capacitors should there be?” Without addressing these questions properly, designers could end up either with an over-designed system and much time-wasted, or under-designed system and facing another redesign. To avoid this situation from occurring, a top-down design approach, similar to [34], is proposed in this chapter. The proposed design approach presents a systematic way of defining system-level parameters such as gain, bandwidth, slew-rate, matching, and etc. Compared to the traditional approach, it separates top-level design from circuit-level optimization. The separation is favorable because it provides designers with insight into system architecture without investing heavily in low level circuitry. The process of designing level circuitry is a tedious and time consuming process, and it would be a complete waste of resource if the low-level circuitry doesn’t meet the product requirement due to inadequate architectural choice. By adopting the proposed approach, designers are provided with not only a way of quickly choosing the suitable architecture, but also detailed specification for low-level circuitry. The top-down design approach, demonstrated in Fig. 4.29, will be discussed next, and its advantages will be presented.

![Figure 4.29 Proposed top-down design methodology](image-url)
The proposed top-down design methodology takes advantage of software package, Matlab. Matlab offers an excellent platform for system level modeling. Within Matlab, pipeline ADC can be modeled by using Simulink, an discrete-time simulator with graphical user interface. A 12-bit one-bit per-stage pipeline ADC is modeled in Simulink, as shown in Fig. 4.30. The model consists of 12 pipeline stages and a DAC. Pipeline stages are cascaded together, with digital output of each stage connected to the ideal DAC. The DAC converts the output of the pipeline ADC back into an analog signal. The reconstructed analog signal can be measured and compared to the analog input signal to indicate the performance of the pipeline ADC.

A basic pipeline stage, shown in Fig. 4.31, contains a relay block (act as a comparator), a summing block, a gain block, and a delay block. The basic pipeline stage is a mathematically identical to that described in Eqn. (4.1). Each block can be further expanded to include non-idealities such as offset, mismatch, and thermal noise. The models for switch thermal noise, capacitor mismatch, opamp DC gain, bandwidth, and slew rate, and comparator offset will be presented in the following sections.
1. Thermal Noise \((kT/C)\)

As discussed before, in a pipeline stage shown Fig. 4.2, each ON-switch is modeled as a combination of noise source, on-resistance \(R_{on}\) and ideal switch. During each clock phase, the noise is sampled onto capacitors \((C_1\) and \(C_2)\), amplified, and passed onto following stages. To account for the effect of thermal noise on the overall pipeline ADC, thermal noise should be modeled, and the model should be included in the ideal model of pipeline stage. In order to simplify the modeling of pipeline ADC stage, it is reasonable to only model the dominant source of thermal noise. As explained before, the dominating source of thermal noise originates from the switch \(S_6\). The noise generated from \(S_6\) is sampled onto capacitors \(C_1\) and \(C_2\) during the sampling phase, thus limiting overall signal to noise ratio. The power of the dominant thermal noise has been shown to be \(kT/C\), where \(C\) is sum of \(C_1\) and \(C_2\). To model switch induced thermal noise, a mathematical description is required. The mathematical description is expressed as

\[
V_{out}(t) = V_{in}(t) + \sqrt{\frac{kT}{C}} \cdot n(t)
\]  \hspace{1cm} (4.56)

where \(k\) is Boltzman’s constant, \(T\) is absolute temperate, \(C\) is the size of hold capacitor \((C=C_1 + C_2)\), and \(n(t)\) is Gaussian random variable. The corresponding Matlab model is shown in Fig. 4.32. In Matlab model, Gaussian random variable is generated with a random number generator. The random variable is then multiplied by square root of \(kT/C\).
which represents \( \text{rms} \) value of noise. As the last step, the product is combined with the input signal to simulate the additive nature of switch thermal noise.

![Matlab model of switch induced thermal noise](image)

Figure 4.32 Matlab model of switch induced thermal noise

2. Capacitor Mismatch
As explained in Section 4.2, capacitor mismatch will result in a deviation from the ideal stage gain. The deviation is random and directly proportional to the mismatch. Due to the random nature of the deviation, a mathematical model of the capacitor mismatch can be obtained by modeling the stage gain with two components: nominal stage gain and mismatch gain. The model is expressed as

\[
A_s = A_s + k_c
\]  

where \( A_s \) is the resulted stage gain, \( A_s \) is the nominal stage gain, and \( k_c \) is the mismatch gain which is a random number adjusted to reflect capacitor mismatch. An implementation of Eqn. (4.57) is demonstrated in Fig. 4.33b. In the implementation, nominal stage gain is the desired stage gain, Two, which is realized with a constant block, \( sgain \). Capacitor mismatch is implemented with a random number generator (in Matlab control program). The generator outputs an array of random numbers, with each number corresponding to the gain deviation resulting from mismatch in each pipeline stage. For example, in Fig. 4.33, a mismatch block, \( mis(2) \), indicates the amount of the gain error in
the second pipeline stage. The final resulting stage gain is obtained by passing the random number and nominal stage gain, $A_s$, through a sum block.

![Figure 4.33 Stage gain due to capacitor mismatch](image)

3. Opamp Gain, Bandwidth and Slew Rate

Finite opamp gain, as demonstrated in Eqn. (4.34), reduces stage gain by a constant factor. To establish a Matlab model of finite opamp gain, a mathematical model is required. The mathematical model, derived from Eqn. (4.34), can be expressed as

$$A_s^\prime = \left( \frac{1}{1 + \frac{1}{A_{op}}} \right) \cdot A_s$$

(4.58)

where $A_s^\prime$ is the reduced stage gain, $A_{op}$ is opamp DC gain, and $A_s$ is ideal stage gain. The Matlab model, shown in Fig. 4.34a, is a straight implementation of Eq. (4.58). Opamp gain, $A_{op}$, is first modeled as a constant block. The modeled opamp gain is inverted, added to an one through a sum block. The sum is then inverted again to obtain the stage gain reduction factor. The final stage gain is achieved by passing both ideal stage gain, $A_s$, and the reduction factor through a product block.

![Figure 4.34 Reduced stage gain due to finite opamp DC gain](image)

Besides finite opamp gain, insufficient opamp bandwidth and slew-rate will also result in the reduction of stage gain. The Matlab model of the opamp bandwidth and slew-rate is
closely based on the analysis of their effect in switched-capacitor in Section 4.3. There are three operating condition which can occur: 1) slew-rate limited operation, 2) bandwidth-limited operation, and 3) first slew-rate limited followed by bandwidth limited operation. These operating conditions are mutually exclusive, and are selected based on the difference between current input voltage and previous output voltage. The overall Matlab model of the opamp bandwidth and slew-rate is depicted in Fig. 4.35a. The model is accomplished by first multiplexing the input variables (Input voltage $V_{in}$, unity gain bandwidth $UGBW$, slew-rate $SR$, sampling rate $F_s$) into a single input array with a MUX block. Then, the input array is fed into a Matlab function block (with function depicted in Fig. 4.35b). The output of the Matlab function block will produce the final output voltage, which takes into account of the input voltage and the desired output voltage, as well as opamp bandwidth, slew-rate, and sampling frequency.

4. Comparator

The comparator is also one of the significant error sources in a pipeline stage, which can be modeled in Matlab. Comparator error, due largely to the existence of the comparator offset, will result in both loss of quantization levels and codes. The loss of quantization levels and codes leads to non-linear distortion in pipeline ADCs. To simplify the
Monolithic Nyquist Rate ADC With Digital Calibration

comparator modeling in Matlab, the offset is assumed to be a random variable [22]. This assumption is valid because the comparator offset is a result of transistor mismatch, which contain a random component. With the offset, the comparator can be described mathematically as

\[
\text{Compare}(V_{in}) = \begin{cases} 
0 & V_{in} \leq V_{th} + V_{offset} \\
1 & V_{in} > V_{th} + V_{offset} 
\end{cases}
\]  

(4.59)

where \(V_{in}\) is the input signal, \(V_{th}\) is the threshold voltage, and \(V_{offset}\) is the random offset voltage. The comparator, implemented in Fig. 4.36a, is realized with a relay block. The relay block is configured, shown in Fig. 4.36b, to include an offset factor, \(offset(2)\), to account for the effect of comparator offset in the second pipeline stage. Generally, the offset factor for the \(i\)th stage, \(offset(i)\), is generated from a random number generator in a Matlab control program.

(a) Matlab model for comparator  
(b) Matlab parameters for comparator

Figure 4.36 Matlab model and parameters for comparator

5. Overall Pipeline Stage

Using Matlab models established above, a complete pipeline ADC stage can be constructed to account for the majority of dominant sources of noise and distortion. The model depends on a handful of variables such as capacitor size, opamp DC gain, bandwidth and slew rate, which can easily optimized by placing the entire pipeline ADC model in a closed loop.
The Matlab model has been used extensively to verify pipeline ADC system architecture and system level optimization in this thesis. The complete pipeline stage model is shown in Fig. 4.37, which use the component models described above. In Matlab, 12 stages have been constructed and cascaded together to form a pipeline ADC. An ideal pipeline ADC’s SNDR plot is shown in Fig. 4.37a, while the SNDR plot generated from a non-ideal pipeline ADC is shown in Fig. 4.38b. In the ideal SNDR plot, it can be observed that the dominant source of error is quantization noise, and a SNDR of 72 dB is achieved. In the case of the non-ideal pipeline ADC, opamps were assumed to have a DC gain of 1000 V/V, a unity-gain bandwidth of 50 MHz, a slew-rate of 50 V/μs, a total capacitance of $C = 5 \text{ pF} \ (C = C_1 + C_2)$, and a 0.1% capacitor mismatch. Clearly, a degradation in SNDR can be spotted in the form of noise and harmonic distortions. The noise floor is elevated from the ideal level shown in Fig. 4.38a, which is contributed by $kT/C$ noise. The harmonic distortion is almost non-existent in the ideal SNDR plot. In the non-ideal SNDR plot, the harmonic distortion is the dominant error, which is a combined product of capacitor mismatch, finite opamp gain, opamp bandwidth and slew-rate, and comparator offset.

![Figure 4.37 Detailed Matlab model of typical pipeline stage](image-url)
4.6 - Conclusion

In this chapter, the work has been concentrated on the design of a 10-bit 2 MSample/s pipeline ADC. A brief introduction on one-bit per-stage pipeline is introduced. The non-idealities associated with the design, such as thermal noise, gain error, comparator offset error are discussed in details.

To correct for comparator offset error, an offset calibration algorithm, adapted from the offset calibration algorithm proposed in Chapter Two, has been proposed. The theory behind the offset calibration is introduced, and the calibration procedure is outlined. In Chapter Five, presented experimental results will demonstrate that the offset calibration algorithm will improve the performance of the pipeline ADC.

Throughout the rest of the chapter, detailed design analyses of pipeline ADCs have been carried out. In addition, a top-down design approach in Matlab and Simulink has been proposed to supplement the design analyses conducted. The prospect design approach separates system level optimization from circuit level design, thus enabling a quick analysis of various architectural and a definition of system level variables.
Chapter 5 - Experimental Results

In Chapter Three and Four, the design and implementation of a flash ADC and pipeline ADC has been presented. The flash ADC and pipeline ADC have been fabricated in TSMC 0.25 μm and 0.18 μm CMOS process, respectively. The fabricated ADCs have been tested in the Mixed-Signal Test Lab in McGill University. In this chapter, the measurement and test results will be presented and discussed.

5.1 - Teradyne Tester Setup

The design of a flash ADC and pipeline ADC has been discussed in detail in Chapter Three and Four. In Chapter Three, a 4-bit flash ADC with digital calibration has been implemented in the TSMC 0.25 μm CMOS process. Unfortunately, the flash ADC did not function as designed due to an internal short. So, instead, a flash ADC has been built with discrete components, and tested. The experimental results will be discussed in full detail in the next section. In Chapter Four, with the aid of the novel offset calibration algorithm, a 10-bit low-power low-voltage pipeline ADC has been implemented in the TSMC 0.18 μm CMOS process. The implementation of the pipeline ADC proved to be functional and experimental results will be discussed in a subsequent section.

The testing of the prototypes has been conducted in The Mixed-Signal Testing Lab at McGill University. This lab is equipped with various testing equipment: Teradyne A567 mixed-signal tester, HP Oscilloscope, Spectrum analyzer, DC source and Multimeter. The
The majority of the testings have been done on the Teradyne A567 mixed-signal tester, which is capable of generating low-frequency high precision analog signals (up to 20 Bits below 500 kHz), sampling analog waveforms with high accuracy, and writing/reading arbitrary digital signals at a frequency of up to 20 MHz. A photograph of this tester is shown in Fig. 5.1.

Figure 5.1 McGill Mixed-signal Tester Lab setup

5.2 - Digital DC Reference Source

The digital DC reference source has been implemented and tested extensively in the MACS laboratory. The majority of the work reported in this section can be found in [2] and [37]. In essence, the study reveals that PDM encoded signals are preferred over PWM encoded signals, as the low-pass filtering requires less silicon area to implement the same quality of signal. This is illustrated in Fig. 5.2 in two slightly different ways. In Fig. 5.2a, we observe the length of time it takes the output signal to reach the desired DC level when a step change in the DC level occurs. The DC level was encoded in the form of a PWM and PDM signal. The low-pass filter was designed such that the RMS value of the AC ripples were attenuated to equal levels. Clearly, the PDM encoded signal reaches steady state much faster than the PWM encoded signal. The study also revealed that when
identical filters are used for both the PDM and PWM bitstreams, the AC ripples from PDM bitstream were significantly smaller. This can be seen from Fig. 5.2b, where two PWM bitstreams and one PDM bitstream are compared.

When the settling time and the RMS value of the AC ripple of the PDM and PWM bitstreams are compared, the PDM bitstream holds a clear advantage: The PDM bitstream can be used to achieve the same AC ripple as PWM, but with a much smaller time constant. A smaller time constant leads to a much smaller resistance and capacitance value. This is significant because smaller silicon area is required for the purpose of DC voltage generation. In addition, a smaller time constant also reduces start-up time for the flash and pipeline ADC designed and implemented in Chapter 3 and 4.

![Graphs showing equal AC ripples and equal time constant](image)

(a) Equal AC ripples

(a) Equal time constant, τ

Figure 5.2 Experimental result of the proposed DC reference generator.

5.3 - Flash ADC

5.3.1 - PCB and Tester Setup

A detailed implementation of 4-bit flash ADC has been discussed in Chapter Three. The proposed 4-bit flash ADC has been fabricated in a TSMC 0.25 μm CMOS process. Due to
an internal short, the fabricated chip was tested and proved to be non-functional. In order to demonstrate the reference mismatch cancellation and offset calibration algorithm introduced in Chapter Three, a 4-bit flash ADC has been implemented with discrete components on a printed circuit board (PCB). A schematic of the PCB implementation of the flash ADC is provided in Fig. 5.3. A photograph of the PCB is demonstrated in Fig. 5.4. The discrete implementation of ADC contains a bank of resistors (280 KΩ each) and capacitors (27 pF each), and four Quad CMOS comparators (TLC374CN from Texas Instrument). The resistance and capacitance values for each DC generator were chosen to ensure a small AC ripple (τ =7.56 μs) when the tester is sourcing a PDM bitstream at 10 MHz. The CMOS comparators were chosen for their high input impedance (10^{12} Ω) as to minimize the loading effect. A comparator with a low input impedance will not only causes an undesired drop in the reference levels, but also couple the input signal into the reference levels.

The PCB implementation of the flash ADC was designed and mounted on the Teradyne A567 mixed-signal tester as shown in Fig. 5.5a. Additional test equipment used to perform the measurements include: an oscilloscope and spectrum Analyzer. The test station set-up is shown in Fig. 5.5b.
Figure 5.3 Schematic of Discrete Flash ADC

Figure 5.4 Details of the flash ADC PCB
5.3.2 - DC Test

For the 4-bit flash ADC, DC tests include the test of reference levels, DNL and INL measurement. These tests are performed under DC condition, and are only an indication of the ADC's performance under static or low-frequency condition.

**Reference Levels**

With the PCB fixture shown in Fig. 5.4, the first step is to generate and measure the DC reference levels. This is performed with the help of the Teradyne Tester. During the test, the Teradyne Tester is configured to simultaneously output 16 digital bitstreams. Each digital bitstream is modulated with a pre-set reference level. All 16 bitstreams are fed into the onboard RC filter through pin $B_1$ through pin $B_{16}$ as shown in Fig. 5.3. Thus, the reference levels are generated as the bitstreams pass through the on-board RC filters. The DC test is then conducted by probing the outputs ($V_1 - V_{16}$ as shown in Fig. 5.3) of all the 16 on-board filters with either an oscilloscope, or the tester.

During the test, the Teradyne tester has been setup to output digital bitstreams with 5.0 V as logic high, and 0.0 V as logic low. The length of PDM bitstream is set to 1024 bits, and the tester generates and outputs each digital bit at a frequency of 10 MHz. In order to investigate the accuracy of the reference levels, 16 bitstreams are selected such that the
corresponding DC levels are separated by only one $\text{LSB}$ (5.0 V / 1024 = 4.88 mV), for example, from 4.88 mV, 9.76 mV, ..., to 78.08 mV. Under this setup, the reference levels are measured and plotted in Fig. 5.6a. The plot shows that the reference levels are monotonically increasing as expected. For the reference test, the 16 bitstreams can be also chosen to correspond to any set of consecutive 16 DC levels, ranging from 0.0 V to 5.0 V. Different set of DC reference levels have been randomly chosen, and tested. All tested sets of DC reference levels demonstrates monotonicity. The monotonicity implies that, if 1024 bitstreams and RC filters are used during DC test, 1024 unique reference levels ranging from 4.88 mV to 5.0 V can be generated. And the generated reference levels will be monotonically increasing. Thus, theoretically, the generated 1024 reference levels can be employed in either a 10-bit ADC, or DAC.

An additional test has been conducted with a bitstream of longer length in an attempt to render reference levels with higher resolution (For example, with 1 $\text{LSB} = 1.22$ mV). This is desirable because it can lead to a ADC or DAC with a higher than 10-bit resolution. A PDM bitstream of length 4096 bits is used, the reference levels plot is demonstrated in Fig. 5.6b. The plot is not monotonically increasing as desired. The result is disappointing, however, it is possible the disappointment is due to limitation of the equipments used and noise.

Figure 5.6 Reference levels generated by the flash ADC
• **DNL and INL**

The accuracy of the reference levels alone can not reflect complete DC performance of ADCs. In flash ADCs, comparators could contribute errors to the ADCs output codes. A more generally accepted DC performance is DNL and INL measurement. With the same fixture shown in Fig. 5.5a, DNL and INL measurements are performed, and the results are discussed next.

Assuming an ideal analog-to-digital converter (ADC) with finite digital codes exactly 1 LSB apart (DNL error = 0) or an ideal digital-to-analog converter (DAC) with analog output values exactly one code apart (DNL error = 0), the DNL error is defined as the difference between the ideal and the measured code transitions for successive codes for an ADC or the difference between the ideal and the measured output value between successive DAC codes. As an example, when using an ADC, as the analog input voltage increases, if the next code transition occurs at a voltage 1.5 LSB away from the current transition, the DNL error is 0.5 LSB; if it occurs at 0.5 LSB away, the DNL error is -0.5 LSB. The INL error is defined as the sum of the DNL errors starting from code 0...00 to the code where the INL measurement is desired.

There are several methods of measuring DNL and INL. The methods include step search, servo method, histogram testing [36], and etc. The step search method has been employed for its simplicity and accuracy with the help of the Teradyne mixed-signal tester. The measurement has been conducted with a triangular wave (both rising and falling ramp are used). During the test, a triangular wave test signal with an amplitude of 5 Vpp and a frequency of 10 kHz is generated from the tester. The signal is then fed into the negative terminal of all on-board comparators, while the 16 tester-generated reference levels are connected to the positive terminal of each comparator. The measured DNL and INL is demonstrated in Fig. 5.7. A maximum DNL of 0.8 LSB and INL of 1.78 LSB were found, where one LSB is equivalent of 4.88 mV.
5.3.3 - AC Tests

DC tests such as DNL and INL usually set an upper limit on the performance of the ADC. With a higher sampling rate and input frequency, the dynamic performance of the ADC typically degrades. Under AC conditions, the performance of ADCs are determined by different sets of measurements. Among the measurements, SNDR is widely quoted. SNDR is defined as the ratio of signal power over the sum of noise and distortion power. The ratio is measured in Decibels (dB). Usually, a higher SNDR is desirable.

To conduct the SNDR measurement for the 4-bit ADCs on the PCB, the PCB and Teradyne tester have been setup in the same fashion as in the DC tests. The tester generates all 16 reference levels, and feeds them into onboard comparators. A sine wave signal is fed into the ADC. The input sine wave has a frequency ranging from 10 Hz to 500 KHz (Tester upper limits), and an amplitude of 40 mV. The ADC has a sampling frequency of 5 MHz. To obtain the SNDR measurement, the ADC is allowed to perform the analog to digital conversion on the input sine wave for a short amount of time. During this time, 1024 converted codes are collected from the output of the ADC with the use of the tester. The output codes are then reconstructed, and the reconstructed waveform is demonstrated in Fig. 5.8a. A 1024-points FFT has been performed on the reconstructed output signal and the results are shown in Fig. 5.8b, where an average SNDR of 23.8 dB
was achieved. The SNDR of 23.778 dB is close to the theoretical limits (25.8 dB) for the 4-bit flash ADC. This SNDR remains constant throughout the entire input sine wave frequency (0 - 500 KHz), as demonstrated in Fig. 5.8c.

![Figure 5.8](image)

**Figure 5.8** Experimentally measured SNDR of the Flash ADC

### 5.4 - Pipeline ADC

The goal of this section is to demonstrate that, through digital offset calibration, the performance of a pipeline ADC can be improved. The design details of the pipeline ADC have been provided in Chapter Four. In Chapter Four, a 10-bit pipeline ADC has been designed and implemented in a TSMC 0.18 μm CMOS process.
The experiments conducted on the pipeline ADC include the measurement of residue signal, comparator offset, stage gain, DNL, INL, and SNDR. Measurements before and after calibration are taken and compared, and performance improvement through digital calibration will be demonstrated.

5.4.1 - PCB and Tester Setup

A two-layer printed circuit board (PCB) was made to facilitate the testing of the pipeline ADC. The PCB contains a tester interface, a socket for the pipeline ADC chip, and two power supply regulators (one for the digital circuitry and one for the analog circuitry). Additional clock and input signal interface are provided through on-board BNC connectors. The experiments have been conducted by mounting the PCB on the DIB of the tester, as depicted in Fig. 5.9. The tester is used to generate test signals and collect output data.

![PCB board and tester setup.](image)

5.4.2 - Stage Residue and Stage Gain

After powering up the circuit, the residue signal generated from the first stage of the pipeline ADC was captured with the tester. The residue signal was first buffered through an on-chip unity gain amplifier placed on the chip exclusively for this purpose. Two types
of measurements are made on the residue signal. The first test, shown in Fig. 5.10a, is conducted with a rising ramp signal as the input signal. It can be seen that the residue signal resembles a PAM signal, where the ramp signal is amplified, modified, and modulated by the sampling clock signal. The second test, shown in Fig. 5.10b, is conducted with an input sinusoidal signal. Similar to the first test, the residue signal appears as an amplified sinusoidal signal beating with the clock signal. If the clock is removed from both residue signals, the modified residue signals are identical as the ones shown in Chapter Four. From the modified residue signals, crucial information such as stage gain can be extracted.

From the captured stage residue shown in Fig. 5.10a, information on stage gain can be extracted. As discussed in Chapter Four, stage gain is a crucial factor in determining the performance of pipeline ADCs. For the pipeline ADC implemented in this thesis, a stage gain of 2.0 V/V is desired. A stage gain other than 2.0 V/V will lead to some form of nonlinear distortion. To measure the stage gain, a rising ramp signal of slope $k_{\text{in}}$ was applied to the ADC input and the slope of the residue signal (after the clock signal is...
removed) was measured. The stage gain can then be obtained from the following expression

\[
\text{StageGain} = \frac{k_{\text{res}}}{k_{\text{in}}}
\]  

(5.1)

The stage gain measurement was performed on 15 different samples of the ADC operating with a sampling clock of 2 MHz. The input ramp signal was set to have a slope of 0.08 V/ms over a voltage range of 0.8 V. The corresponding slope of each residue signal was then measured and the stage gain computed. The results are depicted in Fig. 5.11a, where the average stage gain was 1.998 V/V. As discussed in Chapter Four, stage gain can be affected by capacitor matching, opamp gain, bandwidth, and slew rate limiting. With an average stage gain of 1.998V/V, one can conclude that the combination of capacitor mismatching, opamp gain, bandwidth, and slew rate will contribute to a residue error of less than 1/2 LSB in the first pipeline stage under DC condition. However, as the input signal frequency increases, with finite DC gain and bandwidth, the opamp starts contributing to the stage gain error. It is expected that the stage gain will decrease as the input frequency increases. The experiments have been performed by choosing the input sine wave with various frequencies (10 Hz - 500 KHz), the stage gain is then obtained by measuring the amplitude of the residue signal from the first stage. The results, shown in Fig. 5.11b, demonstrate that the stage gain does not deteriorate significantly (<2%) with the input frequencies up to 500 KHz.
5.4.3 - Comparator Offset

The comparator offset calibration algorithm proposed in Chapter Three can be used to improve the performance of the pipeline ADC. In the case of the pipeline ADC, the calibration algorithm is applied to the first and second stage, as the comparator offset has less of an effect in later stages of the pipeline. Two digital DC reference sources were dedicated for the purpose of DC calibration. Each digital DC reference source was implemented off-chip using the built-in memory capability of the mixed-signal Teradyne tester and several discrete filter prototypes. Various digital bit patterns were clocked out of memory at a clock rate of 10 MHz, passed through an RC filter and applied to first and second stage of the pipeline ADC. Through the digital search algorithm introduced in Chapter Two, a DC level that corrects for comparator offset was applied to each stage.

For example, the comparator offset of the first stage of a pipeline chip was measured to be as much as 98.6 mV. The offset measurement was obtained by setting the negative input to the comparator to the reference voltage of $V_{\text{mid}} = 0.9$ V (mid-range voltage) and applying a ramp signal at the other terminal starting from 0 V. The voltage which causes the comparator output to flip will be noted, as $V_{\text{flip}}$. The offset voltage is calculated by subtracting $V_{\text{mid}}$ from $V_{\text{flip}}$. The measured offset results are shown in Fig. 5.12a, together...

![Figure 5.11 Measured Stage Gain from 15 sample chips](image-url)
with the expected or ideal result. On a side note, the latched comparators used in the implementation of the pipeline ADC have been found to have a relatively large offset (average offset of 32 mV). The presence of a large offset is not surprising, as it is well known that latched comparator have a large offset. Upon applying the calibration algorithm to the chip, and resetting the DC level that appears at the negative input of the comparator, and repeating the offset measurement, we obtain the results shown plotted in Fig. 5.12b. As it is evident, the comparator offset is now approximately 1 mV. And the magnitude of the offset is really limited by the resolution of the DC generator. In this particular case, it was 1 mV. A batch of 15 sample chips were measured and calibrated. The statistics on the magnitude of the comparator offset before and after calibration are plotted in Fig. 5.13. As expected, the calibrated result are all within an LSB of the DC generator.

![Graph showing measured and calibrated comparator offset](image)

(a) Measured comparator offset is 98.6 mV. (b) After calibration, measured comparator offset is 1 LSB.

Figure 5.12 Pipeline MSB stage latched comparator characteristic before calibration and after calibration.
5.4.4 - Pipeline Performance

The performance of the pipeline ADC can be determined through several indicators. These indicators include DNL and INL measurement, SNDR, and Dynamic Range. DNL and INL tests will demonstrate the DC performance, while SNDR and Dynamic Range will demonstrate the AC performance of the pipeline. Both pre-calibration and post-calibration results will be presented and compared to demonstrate the effectiveness of the offset-calibration algorithm.

- DNL and INL

DNL and INL is a static measurement indicating the linearity of the pipeline ADC at DC condition. The method of obtaining DNL and INL is similar to that of the flash ADC. In Fig. 5.14a, a pre-calibration DNL and INL plot is shown, where the maximum DNL is 0.91 LSB, and the maximum INL is 0.83 LSB. Through the use of the offset calibration, the maximum DNL is reduced from 0.91 LSB to 0.25 LSB, and the maximum INL is reduced from 0.83 LSB to 0.23 LSB. The DNL and INL plot after calibration is demonstrated in Fig. 5.14b.
SNDR and SFDR

SNDR provides a measurement of the dynamic performance of the pipeline. For ADCs, the SNDR is defined as the ratio of the RMS value of the sine wave (input sine wave for the ADC) to the RMS value of the noise of the converter from DC to the Nyquist frequency, including harmonic content. It is typically expressed in decibels.

For the pipeline ADC, a high-resolution sine wave, generated from the tester, is input to the ADC. The tester is also used to collect the digital codes from the ADC output. SNDR is then calculated by performing a FFT on the collected digital codes. During the SNDR test, the tester outputs a sampling clock at 2 MHz. This clock signal is used by the ADC as the sampling clock. A coherent input sine wave with a frequency of 121.093 KHz (121.093 kHz / 2 MHz = 31/512) and an amplitude of 0.8 V_{pp} is sampled and converted by the ADC.
into digital binary codes. After collecting the output codes and reconstructing them into a sine wave, a FFT is performed and is shown in Fig. 5.16 and Fig. 5.16. SNDR plot of non-calibrated pipeline ADC is presented Fig. 5.16a, where an average SNDR of 52.3 dB has been achieved. As a comparison, an average SNDR of 59.3 dB has been achieved for the offset-calibrated pipeline ADC. The proposed offset calibration algorithm also improves SFDR performance. The non-calibrated pipeline ADC, shown in Fig. 5.16b, achieved an average SFDR of 54 dB, while the calibrated pipeline ADC achieved an average SFDR of 62 dB. This is shown in Fig. 5.16b.
Dynamic Range Plot

Dynamic range is a measurement of input signal amplitude that a converter can resolve, typically expressed in decibels. For instance, a converter with a dynamic range of 60dB means that it can resolve signals in the range in amplitude from 1x to 1000x. Dynamic range is important in communication applications where signal strengths vary dramatically. The measurement is typically done by incrementing the input signal amplitude, and noting the input signal range where the SNDR is above 0 dB.
In this test, the measurement has been performed with and without offset calibration. The pipeline ADC sampling clock is set to be 2 MHz, and an 121.093KHz input sine wave with an amplitude of 0.8 V_{pp} is the input to the pipeline ADC. The dynamic range plot is demonstrated in Fig. 5.16. It can be seen that the offset calibrated pipeline ADC not only achieves a higher SNDR, but also possesses larger dynamic range.

![SNDR plot: Offset calibrated vs uncalibrated](image)

Figure 5.17 SNDR plot vs input range. Sampling frequency \( f_s = 2 \) MHz.

5.5 - Conclusion

In this thesis, a 4-bit flash ADC has been designed with the digital reference source. The flash ADC is implemented on a printed circuit board (PCB) with discrete components. Experiments have been conducted on the PCB, and the results have been presented in this chapter. The experiments conducted show that the proposed digital reference source can be used in high-resolution ADCs, or DACs. For the pipeline ADCs, a comparator offset calibration algorithm has also been developed. A 10-bit pipeline ADC, implemented with the algorithm, has been implemented, fabricated, and tested. The experiments show that with the offset calibration algorithm, comparator offset has been reduced, higher SNDR has been achieved, and wider dynamic range is possible. The experiments conducted on both the flash ADC and pipeline ADC have shown that the use of the digital DC reference source has been a success.
Chapter 6 - Conclusion

6.1 - Discussion of Results

In this work, a novel offset calibration algorithm has been proposed. The calibration algorithm is capable of reducing reference voltage mismatch and comparator offset in flash ADCs, and reducing error induced by comparator offset in pipeline ADCs. The proposed digital calibration utilizes a key component, digital DC reference source, which can be implemented in standard CMOS process. The digital DC reference source is highly insensitive to temperature and process variation. Further studies in the Microelectronics And Computer Systems (MACS) laboratory have shown that it provides a possible alternative to the traditional band-gap reference. The work of this thesis, being part of ongoing analog microelectronics research in MACS laboratory, was devoted to the study of the underlying principle, limitation, and applicability of the digital calibration using the digital DC reference source.

In Chapter Two, the digital DC reference source, consisting of digital memory and a RC low-pass filter, has been introduced and studied. Experiments conducted show that the proposed digital DC reference source is capable of generating an arbitrary DC level with a AC ripple ~ 1.0 mV. This level of AC ripple can be achieved with a supply voltage of 5.0 V, 2.5 V, or 1.8 V. In Chapter Three, the design of a 4-bit flash ADC using the proposed digital DC reference source has been presented. The digital DC reference source lends itself in reducing mismatch in reference voltages, and calibration of comparator offset.
The design issues related to comparator has been explored. To further investigate the application of the digital DC reference source, a complete pipeline ADC design has been demonstrated in Chapter Four. The same calibration algorithm, employed in Chapter Three, has been adapted to the design of a 10-bits pipeline ADC. Finally, experiments conducted on the digital reference source, the flash ADC, and the pipeline ADC have been presented, and the results have been discussed. The experimental results show that the proposed calibration is capable of improving ADCs' performance.

In conclusion, this work has demonstrated that the application of the digital DC reference source in flash ADCs and pipeline ADCs. The digital DC reference source and the proposed calibration algorithm proves to be an efficient and attractive method in improving ADCs' performance.

6.2 - Future Directions

As future research, the flash ADC implemented in the Chapter Three can be improved to be area and power efficient. The possible improvements were detailed in the chapter. In addition, the comparator offset calibration has been carried out with external components (the mixed-signal tester). The digital DC reference source could be fully integrated with the pipeline ADC, which will help to reduce noise and AC ripples, and improve the pipeline ADC performance.
References


Monolithic Nyquist Rate ADC With Digital Calibration


