Signal Integrity Analysis of Transmission Lines Backed by Electromagnetic Bandgap Structures in High-Speed Systems

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Last but not least, I would like to thank my parents for always being there supporting me and giving me unconditional love. This work is dedicated to them.
ABSTRACT

Signal integrity in transmission lines routed above an Electromagnetic Bandgap (EBG) structure is investigated in this thesis. The EBG structure can be designed to induce a wide omni-directional stopband and when it is employed in a conventional parallel plate power distribution network (PDN), efficient suppression of power/ground or simultaneous switching noise is provided. However, the signal lines that are routed above the EBG structure see an interrupted return current path. To investigate this loading effect, a number of signal routing scenarios in a PDN with an embedded mushroom-type EBG structure are investigated through full-wave simulations. Also, a sample prototype based on one of the routing scenarios was fabricated and characterized in frequency and time domain measurements by S-parameters and the output eye diagrams. Furthermore, an equivalent lumped-element circuit is developed to represent the EBG return path. This model is further developed to be applicable to the studied routing scenarios and can be easily incorporated in commercial circuit simulators. The proposed models enable rapid signal integrity analysis as well as global system simulations. Verified by both simulation and measurement results, the signal integrity characteristics of the signal lines backed by an EBG structure are degraded. In order to improve the quality of signal transmission, a modified configuration is introduced. This solution, which utilizes a solid conductor island in the EBG reference plane, offers an optimal insertion loss profile while maintaining noise suppression characteristics of the embedded EBG structure in the PDN.
Lintégrité des signaux sur les lignes de transmission au dessus de structures électromagnétiques de bande interdite (EBI) est investiguée dans ce mémoire. Les structures EBI peuvent être conçues afin dinduire une bande atténuée omnidirectionnelle large et quand employées dans un réseau de distribution de puissance (RDP) conventionnel de lames à faces parallèles, une suppression efficace du bruit associé à louverture et fermeture électronique d’un circuit de puissance est réalisée. Cependant, les lignes de signaux au dessus dune structure EBI sont sujettes à un chemin de retour de courant interrompu. Pour investiguer cet effet de chargement, quelques scénarios de cheminement de signaux dans un RDP avec une structure EBI de type champignon embarqué sont étudiés par des simulations dondes-complète. De plus, un des prototypes a été fabriqué et caractérisé dans le domaine fréquentiel et temporel en utilisant les paramètres de dispersion et des diagrammes en oeil. Également, un modèle de circuit à constantes localisées représentant le chemin de retour du EBI a été développé. Ce modèle a également été poussé afin dêtre utilisable dans les scénarios de cheminement de lignes et peut être facilement incorporé dans des simulateurs de circuits commerciales. Les modèles proposés permettent une analyse rapide de lintégrité des signaux ainsi que des simulations globales de systèmes. Vérifié par des simulations et des mesures expérimentales, les caractéristiques de lintégrité des signaux des lignes supportées par une structure EBI sont dégradées. Afin d’améliorer la qualité des signaux de transmission, une configuration modifiée est introduite. Cette solution, utilisant une île de conducteur solide dans le plan de
référence EBI, offre un profile d'affaiblissement d'insertion optimal tout en maintenant les caractéristiques de suppression du bruit des structures EBI dans un RDP.
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<th>Description</th>
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<tr>
<td>1-D</td>
<td>One-Dimensional</td>
</tr>
<tr>
<td>2-D</td>
<td>Two-Dimensional</td>
</tr>
<tr>
<td>3-D</td>
<td>Three-Dimensional</td>
</tr>
<tr>
<td>DUT</td>
<td>Device Under Test</td>
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<tr>
<td>EBG</td>
<td>Electromagnetic Band-Gap</td>
</tr>
<tr>
<td>EMI</td>
<td>Electromagnetic Interference</td>
</tr>
<tr>
<td>EMC</td>
<td>Electromagnetic Compatibility</td>
</tr>
<tr>
<td>FDFD</td>
<td>Finite-Difference Frequency-Domain</td>
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<tr>
<td>FEM</td>
<td>Finite Element Method</td>
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<tr>
<td>HIS</td>
<td>High Impedance Surface</td>
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<tr>
<td>NRZ</td>
<td>Nonreturn-to-Zero</td>
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<tr>
<td>PBC</td>
<td>Periodic Boundary Condition</td>
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<tr>
<td>PCB</td>
<td>Printed Circuit Board</td>
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<tr>
<td>PCM</td>
<td>Pulse Code Modulation</td>
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<tr>
<td>PDN</td>
<td>Power Distribution Network</td>
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<tr>
<td>PEC</td>
<td>Perfect Electric Conductor</td>
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<tr>
<td>PMC</td>
<td>Perfect Magnetic Conductor</td>
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<tr>
<td>PPW</td>
<td>Parallel-Plate Waveguide</td>
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<tr>
<td>PRBS</td>
<td>Pseudo-Random Binary Sequence</td>
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<tr>
<td>PSD</td>
<td>Power Spectral Density</td>
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<tr>
<td>P.U.L.</td>
<td>Per-Unit-Length</td>
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<tr>
<td>SSN</td>
<td>Simultaneous Switching Noise</td>
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<tr>
<td>SMA</td>
<td>Surface Mount Adapter</td>
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<tr>
<td>TE</td>
<td>Transverse Electric</td>
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<tr>
<td>TEM</td>
<td>Transverse Electromagnetic</td>
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<tr>
<td>TL</td>
<td>Transmission Line</td>
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<tr>
<td>TM</td>
<td>Transverse Magnetic</td>
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1.1 Overview and Motivations

Electronic systems following Moore's law [1] and Nielson’s law [2] have evolved tremendously during the past decade: Downscaling of the semiconductor devices has enabled doubling the number of the transistors per chip by every 18 months while also allowing for a continuous increase of the operating frequencies and lowering the supply voltages. In response to the ever-growing market demand for increased speed and bandwidth in consumers internet and communication services, a new generation of high-speed highly integrated electronic products has emerged, which supports high data-rate applications such as high-quality video transmission. Distribution of supply voltages in these high-speed and highly-integrated systems is not a trivial engineering task. Lower supply voltages and reduced oxide thickness of modern CMOS technologies have increased the sensitivity of the electronic circuits to any DC power supply fluctuation. As a result, designing the power distribution network (PDN) to provide stable DC supplies and devising methods to suppress voltage fluctuations on the PDN have become a critical part in the engineering of modern electronic systems.
The PDN in a typical electronic system usually consists of power and ground layers, decoupling capacitors and a voltage regulator module as shown in Figure 1–1. Since the power and ground planes in this simple PDN form a parallel-plate waveguide, they are also referred to as a parallel-plate PDN. IC chips and packages mounted on the surface of the board receive their supply voltage from the board level PDN while also containing their internal power distribution network composed of parallel plate power and ground planes. Vias are used for routing the DC supplies through multiple layers. When a device switches, a time-varying current flows through the connecting pins and vias, this current induces fluctuation on the reference voltage planes which is perceived as power/ground noise [3]. If a large number of devices switch at the same time, the overall created fluctuations become more significant and this phenomenon is known as the simultaneous switching noise (SSN) [4]. Power/ground noise or SSN can cause false switching and malfunctioning in digital and analog circuits. Due to the parallel-plate waveguide nature of the PDN, the induced noise propagates in the system and can easily couple to other circuits and lead to electromagnetic interference (EMI), signal integrity and electromagnetic compatibility (EMC) problems [5]. Therefore, design engineers use various techniques to analysis and simulate the PDN in order to predict the signal integrity and EMI issues.

Often, the electrical behavior of a system-level PDN such as the one shown in Figure 1–1 is described with equivalent circuits to enable global system simulations. In [6], a very simplified model for the system shown in Figure 1–1 is suggested to explain the behaviour of PDN. This equivalent circuit is shown in Figure 1–2.
order to avoid large voltage drop at the load, the impedance of the PDN \((Z)\), which is quite frequency-dependent, needs to stay very small over the entire bandwidth of the signal compared to that of the circuit load, i.e. load seen at the point of connection to the chip [7]. In this way, even a large switching current in the PDN will not cause a significant voltage drop across the PDN [8].

Figure 1–2: Equivalent circuit model for power distribution network.
Therefore, the typical techniques to suppress the SSN are realized by minimizing the impedance of the PDN. At low frequencies, the parallel-plate PDN acts as a capacitor [6]. As frequency goes up, the inductance of the connecting paths and leads cause resonance peaks, and therefore the SSN problem is traditionally considered as an inductance problem [9]. A common approach to minimize the impedance resonances and suppress the SSN is by adding decoupling capacitors on the chip, package and board [7]. In high speed applications, dozens of discrete decoupling capacitors are mounted around a sensitive pin of an IC to provide a low impedance path for the voltage fluctuations [10]. However, the effective operating range of this technique is limited to below few hundred MHz due to the self-resonance of the discrete decoupling capacitors. Embedded decoupling capacitors can extend the frequency range up to 1 GHz by utilizing an embedded power/ground pair with high relative permittivity dielectric performing as a capacitor [11]. In this case, not only the effective operating range is still limited, but also its usage is restricted by the expensive fabrication process.

![Top View and side view of the Mushroom-type EBG structure.](image)

Figure 1–3: Top View and side view of the Mushroom-type EBG structure.
To stifle the power/ground noise over a wide operating range, electromagnetic bandgap (EBG) structures, have been introduced recently as a wideband, omnidirectional noise suppression solution [3, 12, 13]. The EBG structures utilized in this application are 2-D periodic configurations which induce stopbands in all azimuthal directions and prevent noise propagation. The most common type of EBG structure used for this purpose is the mushroom-type geometry shown in Figure 1–3. The mushroom-type EBG structure was first proposed by Sievenpiper to block surface currents in order to improve the radiation efficiency of printed antennas [14]. In noise suppression applications, the mushroom-type EBG structure is incorporated in the parallel-plate PDN by replacing one of the power/ground layers as shown in Figure 1–4. For the convenience of expression, a parallel-plate PDN which contains an embedded EBG structure is referred to as an EBG-PDN throughout this thesis.

Figure 1–4: Power distribution network with embedded mushroom-type EBG structure.
Since the mushroom-type EBG structure was introduced into the power distribution networks, extensive research has been carried out in this field. Most recent research explorations focus on two aspects. One is extending the lower edge of the stopband to below 1 GHz and creating a wider stopband. This objective is realized by geometry modification to increase the effective inductance of the structure, such as by using meander lines to connect patches [15] and adding more vias in each cell [16, 17]. The other direction of research in this area is minimizing the size of the EBG structure to adapt it to packaging and integrated circuit form factors. Preliminary results in miniaturizing an EBG structure have been achieved by using high-k dielectric substrate [18, 19]. Nonetheless, there is a third aspect in the application of EBG-PDNs, which is evaluation of EBG impact on signal integrity and interconnect routing. This topic is studied in this thesis.

When signal lines are routed within an EBG-PDN, they are partly referenced to a patterned metallic surface. In this case the signal integrity could be considerably degraded due to the inevitable discontinuities in the return current path. The discontinuities in the return current path, such as vertical vias and plane splits, not only change the impedance of the signal line which in turn results in signal reflection [20], but also can support resonance modes of the power/ground planes and contribute to the radiated field emission [21]. In fact, signal integrity degradation has been studied in several recent publications for various EBG-PDNs [3, 22–26]. In [3], increased reflection noise and impedance variation is noted in the output of a trace reference to a mushroom-type EBG structure and is compared to the conventional
case of a parallel-plate PDN without the EBG structure. Similar results are found for different EBG geometries such as L-bridged EBG structure in [23], meander-line EBG structure in [24], AI-EBG structure in [25] and EBG structure with triangular and hexagonal arrays in [22]. In the designs reported in [3, 26], significant transmission loss is observed above the bandgap, while within the bandgap an acceptable signal transmission quality is maintained. It can be concluded that the signal degradation problem in interconnects routed inside an EBG-PDN becomes more and more significant as the date rates and signal bandwidths increase.

The impact of the EBG surface on signal integrity has been mostly monitored in the time domain at data rates below 3 Gb/s where the bandwidth does not overlap with the higher frequency resonances induced by the EBG structure [3, 22–25]. In [23], the authors suggest using shorter signal lines and data rate below 3 Gb/s to maintain signal integrity. In [24], differential signalling is recommended while in [22] the signal is routed in another layer by adding an extra metal plane as shown in Figure 1–5. All of these methods either sacrifice the system performance or increase the design complexity and fabrication cost. A practical solution to improve the signal integrity of the interconnects in EBG-PDNs of high-speed systems is definitely needed.

Another important issue that needs to be addressed is global system simulations when an EBG-PDN is used. Due to the different scales of the components in a system, it is extremely costly to conduct global simulations by using conventional
full-wave methods such as finite element method (FEM) and finite-difference time-domain (FDTD) [27]. In order to enable global system-level simulation, an equivalent circuit for the EBG-PDN structure is needed, which should be compatible with common circuit solvers such as SPICE simulator. This model must also provide a fast and accurate estimate of the stopband and its impact on signal integrity. To date, several circuit models have been proposed for the mushroom-type EBG structure and parallel-plate PDN but none has been integrated in a system simulation. For example, in [14], a parallel L-C resonator model is given to predict the approximate center frequency of the bandgap. Note that there are no parallel-plate power/ground pair in the studied antenna design and this model is not suitable to represent EBG-PDNs. In [28], a lumped-element equivalent circuit is introduced to predict the stopband of the mushroom-type EBG structure embedded in parallel-plate waveguide, i.e. an EBG-PDN, but it has not been extended to include the embedded interconnect in the EBG-PDN. The model proposed in [29] uses the RLGC transmission line model to represent the EBG-PDN and the embedded interconnects. This model can be
considered complex and it loses accuracy in capturing the resonances in the transmission loss profiles, so it needs improvement.

1.2 Objectives and Thesis Contributions

The main goal of this thesis is to investigate signal integrity of interconnects embedded in modern parallel-plate PDNs that contain mushroom-type EBG structures. Mushroom EBG structure is one of the popular solutions for wideband suppression of power/ground noise in parallel-plate PDNs. When signal lines are in such a PDN, the return current path is impaired due to the discontinuities introduced by the mushroom EBG structure such as the splits between the patches and the vias loading the patches. These discontinuities can induce serious signal integrity problems such as waveform distortion and transmission loss. Full-wave simulations and prototype measurements are needed to characterize the potential problems.

This study should first include investigation of the possible routing scenarios of signal lines embedded in such PDN configuration. One of the goals in the design of modern electronic systems is to create compact and highly integrated systems and to make use of all possible substrate layers for routing interconnects. When a mushroom EBG is considered as two dielectric layers dedicated to the PDN, it can raise the criticism of adding fabrication layers. The solution is to utilize these layers for signalling as well. Nonetheless, careful attention should be paid to signal integrity problems due to the interruption in the signal return path. Hence, a few cases of routing are
investigated herein. Each case is analyzed by using full-wave simulations, and evaluated in the frequency and time domains. One of the routing scenarios is fabricated and the quality of signal transmission is evaluated by measuring S-parameters and eye-diagrams.

Furthermore, in order to enable global simulation and speed up simulation time, compact and accurate equivalent circuits are needed for those complicated PDN structures. In this thesis, these models are developed for each routing scenario. The circuit elements of the models are calculated using closed-form formulas with some approximations to directly relate the geometrical parameters of the EBG-PDN to circuit element values. The accuracy of the developed models are validated with full-wave simulations of insertion loss profiles.

The final objective of the thesis is to optimize the EBG-PDN structure in order to improve the signal integrity characteristics of the embedded interconnects while maintaining the noise suppression features of the PDN. In this thesis, a modified mushroom-type EBG configuration is proposed, which contains a continuous conductor trace underneath the signal line. This trace is like a solid conductor island on the EBG surface; hence, it is called the island-EBG for easier explanation. This solid conductor segment is connected to the ground plane by two vias and provides an uninterrupted return current path for the signal. It is shown in this thesis that
the island-EBG structure provides superior signal integrity performance like a conventional stripline while offering effective noise suppression characteristics.

A summary of thesis contributions following the aforementioned objectives are listed herein:

- First time investigation of various routing scenarios in parallel-plate PDNs containing a mushroom-type EBG structure (referred to as an EBG-PDN)

- Development of equivalent circuits for interconnects embedded in the EBG-PDN. These models can be ported to spice-like circuit simulators and enable global system simulations.

- Experimental evaluation of an embedded interconnect in an EBG-PDN in time and frequency domains

- Proposition of a new structure for preserving the signal integrity of interconnects embedded in an EBG-PDN. This modified PDN is referred to an island EBG-PDN in this thesis.

- Experimental evaluation of an embedded interconnect in an island EBG-PDN in time and frequency domains for the first time.
1.3 Thesis Outline

This thesis is organized as follows:

Chapter 2 discusses the background concepts of the signal and power integrity which are presented throughout the thesis. It includes representation of PDN using parallel-plate waveguides and cavity models, as well as describes the design concepts behind a PDN with an embedded EBG structure. Characterization of the EBG structures, specifically the mushroom-type EBG structure, along with practical considerations in fabrication of a PDN containing a mushroom-type EBG structure, are also discussed.

A few signal routing scenarios in an EBG-PDN are investigated in Chapter 3. Full-wave simulations are performed, and S-parameter results and the plots of surface current on the return path are used to compare for various cases. A prototype based on one of the studied cases is fabricated, and the measured transmission coefficient of this interconnect is presented. In addition, the signal integrity performance of the fabricated prototype is evaluated in time domain through eye diagram measurements at various data rates.

Chapter 4 covers the development of the equivalent circuits representing signal lines routed in a mushroom-type EBG-PDN. 1-D and 2-D circuits are used to model various routing cases and the formulas for calculation of the element values are presented. The $S_{21}$ results of the simulated cases are studied, and a reasoning based on
the developed models is provided to describe the dips in the insertion loss profiles. Circuit simulations are compared with full-wave results, which demonstrates an excellent agreement.

In Chapter 5, the design of the Island-EBG is fully described. Both signal integrity and noise suppression performance in this modified EBG-PDN are evaluated using full-wave simulations. The results of the experimental evaluation of this design in time and frequency domains are presented in this chapter. The generated insertion loss and output eye diagram are compared with those of an interconnect embedded in an EBG-PDN without the island conductor strip structure.

Finally, conclusions and suggestions for future work are provided in Chapter 6 of the thesis.
CHAPTER 2
Fundamentals of EBG-PDNs

This chapter reviews the background concepts used in the development of this thesis. The fundamental methods of analysis of a parallel-plate power distribution network are discussed in Section 2.1, which include modelling as parallel-plate waveguide or cavity. This is followed by describing the characteristics of the transmission line in parallel-plate waveguides. In Section 2.2, the origins of the simultaneous switching noise (SSN) are reviewed. The discussion of the SSN frequency spectrum is also provided in this section. The typical simulation methods used to characterize the performance of the EBG-PDN is given in Section 2.3. The mushroom-type EBG structure and its practical applications in parallel-plate PDNs are introduced and analyzed in detail in Section 2.3.

2.1 Power/Ground Planes

In integration of any electronic system, a common platform such as a printed circuit board is needed to mount various circuit components as well as route signals and reference voltages. As electronic systems become more compact, more complex and use a higher number of components, routing networks become highly complicated and 3-D integration methods needs to be used. Multi-layer printed circuit
boards and packages utilize vertical interconnects, i.e. vias, to route signals, power and ground from one layer to another. Figure 2–1 shows the diagram of a typical printed circuit board (PCB) with multi-layer routing.

![Figure 2–1: A multi-layer printed circuit board with vias.](image)

Modern electronic system designers recommend employing solid conductor planes for distribution of power and ground voltages [30]. Overall, a power distribution network (PDN) includes these planes, vias, the connecting pads, traces and pins. In high-speed and high-frequency systems, PDN, in addition to supplying reference voltages, plays a vital role in maintaining signal and power integrity. Moreover, the power distribution network stores and delivers the charges needed for circuits to switch [31]. More recently, the PDN has been perceived as a distributed network which in addition to its DC supply delivery tasks across the system, can support propagation of noise contribute to unintentional electromagnetic emissions [32]. The recommended configuration for a PDN, which places power and ground plane close to each other, has shown to provide benefits in reduction of the electromagnetic interference (EMI) and PDN path inductance [33]. This configuration which includes two conducting layers, one for supply voltage $V_{DD}$ or power, and one for the reference
ground, can be found on chip and package substrates and PCBs.

2.1.1 Parallel Plate Waveguide

The two layers of solid power and ground planes form a parallel plate waveguide, as shown in Figure 2–2. The parallel plate waveguide supports transverse electromagnetic (TEM), transverse electric (TE) and transverse magnetic (TM) mode [34]. The TEM waves refer to the case that there are no field components in the direction of propagation, which are excited and supported by parallel plate waveguide at all frequencies. TE and TM waves correspond to the cases where there are no electric or magnetic field in the direction of propagation, respectively. The cut-off frequency for both $TE_n$ and $TM_n$ mode can be defined as

$$f_c = \frac{n}{2d\sqrt{\mu\varepsilon}}$$  \hspace{1cm} (2.1)
where $d$ is the thickness of the parallel-plate waveguide, $\mu$ is the permeability, and $\varepsilon$ is the permittivity of the dielectric material. In general, TEM is the dominant mode, $TE_n$ and $TM_n$ constitute the higher order modes. The expressions describing the EM fields of a parallel-plate waveguide can be found in [34], which are not repeated here for brevity.

Considering an example of parallel-plate waveguide with the thickness of 2 mm, it can be calculated from Equation 2.1 that the cut-off frequency of the lowest order $TE_n$ and $TM_n$ mode is beyond 10 GHz. Generally speaking, the vertical dimension of practical PCB applications is in several mm approximately [27]. Therefore, only TEM mode is of design concern in many common high-speed systems that operate below 10 GHz.

2.1.2 Cavity Modelling

The analysis of parallel-plate PDN are commonly performed with full-wave electromagnetic simulation tools, analytical solutions or SPICE-based models. Full-wave method are the most accurate and can take into account the arbitrary geometries of PDN, however, at a higher computational cost for complex structure. Simple symmetric structures, like the parallel-plate PDN, are often analyzed using the parallel-plate waveguide model or a resonant cavity model.

In parallel-waveguide model, the plates are assumed to have infinite length in the $z$ direction (Figure 2–2). In the practical PCB systems, the width and the length
of the power/ground planes are few centimeters, or even smaller in the case of new system on package devices. In this situation, waves reflect back and forth from the edges of the board/substrate, creating the resonant cavity modes [35]. The standing wave pattern resulted from cavity resonance produces high-impedance peaks, which block the signal return current at reference planes and therefore impair the signal integrity [36].

![Cavity resonator model with electric field distribution.](image)

Figure 2–3: Cavity resonator model with electric field distribution.

The voltage distribution of the cavity modes in a parallel plate waveguide can be found by solving the 2-D Helmholtz equation with respect to the $x$ and $y$ direction. As boundary conditions, the top and bottom conductor planes are assumed perfect electric conductors (PEC) and sidewalls as perfect magnetic conductors (PMC). The voltage distribution $V(x, y)$ due to the excitation by a filamentary current $I_0$ at the location $(x_0, y_0)$, as shown in Figure 2–3, is given by the Green’s function [37] as follows.
\[
\frac{V_z(x,y)}{I_0(x_0,y_0)} = \sum_{m=0}^{\infty} \sum_{n=0}^{\infty} A_{mn} \cos(k_{xm}x) \cos(k_{yn}y)
\]  

(2.2)

with

\[
A_{mn} = \frac{j\omega\mu d}{ab} \frac{K_{mn}}{k_{xm}^2 + k_{yn}^2 - k^2} \cos(k_{xm}x_0) \cos(k_{yn}y_0)
\]

(2.3)

\(K_{mn} = 1\) if \(m = n = 0\), \(K_{mn} = 2\) if \(m = 0\), \(n \neq 0\) or \(m \neq 0\), \(n = 0\) and \(K_{mn} = 4\) if \(m \neq 0\), \(n \neq 0\). The imaginary unit is \(j = \sqrt{-1}\) and \(k_{xm} = m\pi/a\), \(k_{yn} = n\pi/b\) are the discrete eigenvalues with integer mode numbers \(m\) and \(n\) related to the \(x\)- and \(y\)- directions, respectively. The wave number is \(k = \omega\sqrt{\varepsilon\mu}\) for a lossless structure.

For a low loss case, the wave number is associated with the quality factor, \(Q\), which is determined from the conduct or dielectric losses as explained in [37]. In this case, the wave number is calculated from

\[
k = \omega\sqrt{\varepsilon\mu} \left[ 1 - \frac{j}{2Q} \right] = \omega\sqrt{\varepsilon\mu} \left[ 1 - \frac{j}{2} \left( \tan \delta + \frac{1}{d\sqrt{\pi f \mu\sigma}} \right) \right]
\]

(2.4)

The cavity resonance frequencies for both cases are calculated using

\[
f_{mnp} = \frac{1}{2\pi\sqrt{\varepsilon\mu}} \sqrt{\left( \frac{m\pi}{l} \right)^2 + \left( \frac{n\pi}{w} \right)^2 + \left( \frac{p\pi}{d} \right)^2}
\]

(2.5)

where the length, width and thickness of the cavity are \(l\), \(w\), \(d\), respectively, and \(m\), \(n\), \(p\) are mode number taking the values of 0,1,2,...
For the practical PCB configurations considered in this thesis, the thickness $d$ of the parallel-plate waveguide is much smaller than the plane dimensions $a$, $b$, and only $TE_{mn0}$ and $TM_{mn0}$ modes need to be considered. Therefore, the Equation 2.5 can be modified as:

$$f_{mn} = \frac{1}{2\pi} \sqrt{\frac{\mu \varepsilon}{w}} \sqrt{\left(\frac{m\pi}{w}\right)^2 + \left(\frac{n\pi}{l}\right)^2}$$  \hspace{1cm} (2.6)$$

From Equations 2.2, the voltage distribution $V(x, y)$ for different resonant modes are determined in [21] and are shown here in Figure 2–4.

![Figure 2–4: Distribution of voltage magnitude in a parallel-plate structure for resonant modes of (1,0), (0,1), (1,1) and (2,1) [21].](image)

From Equation 2.5 and 2.6, it can be observed that the resonance frequencies shift to lower spectrum as the dimensions of the cavity increase. For example, a printed circuit board with the volume of $100 \text{ mm} \times 100 \text{ mm} \times 2 \text{ mm}$, made with FR4 substrate with dielectric constant of $\varepsilon_r = 4.4$, shows resonances at 700 MHz.
and 1 GHz due to $TE_{100}$ and $TE_{110}$ modes, respectively.

### 2.1.3 Embeding Transmission Lines in Parallel-plate PDNs

A signal line should provide an efficient and non-dispersive channel for data transmission. To achieve this objective, the mode of propagation in the signal interconnect should be TEM or Quasi-TEM. In this case, propagation constant or phase constant ($\beta$) is a linear function of $\omega$. In the presence of conductor and dielectric losses, when inhomogeneous dielectric mediums are used, hybrid modes with components of E or H field along the direction of propagation are excited. In this case, the mode of propagation is no longer a pure TEM. When considerable conductor or dielectric losses exist, the transmission line becomes dispersive and $\beta$ is no longer a linear function of $\omega$. To capture these characteristics of the lossless and lossy transmission lines, lumped-element circuit model shown in Figure 2–5 is often utilized.

![Lumped-element equivalent circuit for an incremental length of transmission line.](image)

Figure 2–5: Lumped-element equivalent circuit for an incremental length of transmission line.

Where $R$, $L$, $G$, $C$ are per unit length quantities defined as follows:

- $R =$ series resistance per unit length, in $\Omega/m$.
- $L =$ series inductance per unit length, in $H/m$. 

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• \( G \) = shunt conductance per unit length, in \( S/m \).
• \( C \) = shunt capacitance per unit length, in \( F/m \).

Other important properties of transmission line, such as characteristic impedance \( Z_0 \) and propagation constant \( \gamma \), can also be described with \( R, L, G, C \) parameters using the well-known telegraphist equations.

The propagation constant of a transmission line is found from:

\[
\gamma = \sqrt{(R + j\omega L)(G + j\omega C)} \quad (2.7)
\]

The characteristic impedance is related to the propagation constant, which is described as

\[
Z_0 = \frac{R + j\omega L}{\gamma} = \frac{\gamma}{G + j\omega C} = \sqrt{\frac{R + j\omega L}{G + j\omega C}} \quad (2.8)
\]

Finding the per unit length (P.U.L) model for all types of interconnects is not a straight-forward procedure. In general, closed-form formulas for the symmetric and homogeneous structures are available. When a signal line is embedded in a parallel-plate PDN, a stripline geometry is created. Stripline is a TEM transmission line that is widely used for the advantages of easy integration and reduced susceptibility to external EM fields. A thin conducting strip with the width of \( W \) is normally centered between the two conducting planes on top and bottom that have the separation of \( b \)
A stripline with a lossless homogeneous dielectric is a non-dispersive interconnect. It can support higher order TM and TE modes, but these are usually avoided in practice [34].

Derivation of P.U.L. R, L, G and C parameters for a stripline from field relations is not as simple as the case of parallel-plate transmission lines and coaxial lines. Therefore, in practice, simple closed-form formulas developed by curve fitting to the exact solutions are used [34]. The impedance of the symmetrical stripline shown in Figure 2–6 is given as:

$$Z_0 = \frac{30\pi b}{\sqrt{\varepsilon_r} W_e + 0.441b}$$  \hspace{1cm} (2.9)
\[ \frac{W_e}{b} = \frac{W}{b} - \begin{cases} 
0 & \text{if } \frac{W}{b} > 0.35, \\
(0.35 - \frac{W}{b})^2 & \text{if } \frac{W}{b} < 0.35. 
\end{cases} \]

In many practical routing structures, the center strip is not symmetrically located with respect to the top and bottom ground planes. This type of interconnect is referred to as a symmetrical stripline or offset stripline. As shown in Figure 2–7, the signal line is closer to one of the conductor planes. Therefore, there is a stronger field between the line and the bottom ground which acts as the more dominant path for the return current.

![Figure 2–7: Geometry of offset stripline.](image)

The characteristic impedance of the offset stripline given by Robrish in [38] is derived by using a conformal mapping technique. The rectangular cross section of the inner conductor is approximated by an equivalent circle with the diameter of \(d_0\) calculated from:

\[ d_0 = \frac{2}{3}(0.8W + T) \quad (2.10) \]
where $W$ and $T$ are the width and thickness of the strip, respectively.

Then, the characteristic impedance of the offset stripline is defined as:

$$Z_0 = \begin{cases} \frac{\eta_0}{2\pi\sqrt{\varepsilon_r}} \cosh^{-1}(A) & \text{if } \frac{W}{B-T} < 0.35, \\
\sqrt{\varepsilon_r} \left( \frac{W}{B} + \frac{W}{\beta + \gamma} + \frac{2C'_f}{\varepsilon_0} \right) & \text{if } \frac{W}{B-T} > 0.35. \end{cases}$$

where

$$A = \sin\left(\frac{\pi C_L}{B}\right) \coth\left(\frac{\pi d_0}{2B}\right) \quad (2.11)$$

An auxiliary parameter $C'_f$ is used in $Z_0$ formula which is:

$$C'_f = \frac{\varepsilon_r\varepsilon_0}{\pi} \left[ 2\ln\left(\frac{1}{\gamma(\beta - \gamma)}\right) + \frac{1}{\gamma(\beta - \gamma)} \left\{ F\left(\frac{T}{2B}\right) - F\left(\frac{C_L}{B}\right) \right\} \right] \quad (2.12)$$

where

$$C_L = H + \frac{T}{2} \quad (2.13)$$

$$\gamma = \frac{C_L}{B} - \frac{T}{2B} \quad (2.14)$$

$$\beta = 1 - \frac{T}{B} \quad (2.15)$$

$$F(x) = (1 - 2x)[(1 - 2x)\ln(1 - x) - x\ln x] \quad (2.16)$$
2.2 Simultaneous Switching Noise (SSN)

SSN is a voltage fluctuation on the PDN that is induced by the current changes due to the switching of a large amount of circuits at the same time [9, 39]. In essence, the simultaneous switching noise is the simultaneous generation of delta-I noise or power/ground noise. Delta I noise, as explained in [40], is attributed to the voltage drop across the parasitic inductors in the power/ground distribution path, \( L_{\text{eff}} \frac{di}{dt} \), where \( i \) is the surge current or switching current and \( L_{\text{eff}} \) is the effective inductance in the power distribution path.

The \( L_{\text{eff}} \) is found from the inductance of the interconnecting vias, chip wire bonds and the loops created in routing power and ground traces [41]. The SSN voltage is obtained by knowing the number of gates switching at the same time, \( N \), and the rate of current change, \( \frac{di}{dt} \).

\[
V_{\text{SSN}} = NL_{\text{eff}} \frac{di}{dt}
\]

In the path of power/ground voltage delivery, vias are often used in multilayer printed circuit boards to transit a line from one layer to another. Mostly vias are directly routed through the reference voltage planes. They can easily excite parallel-plate waveguide modes and resonance cavity modes that greatly change the impedance of the power/ground planes. Modern studies of power/ground noise in addition to \( L_{\text{eff}} \frac{di}{dt} \) effect include the effect of the parallel-plate PDN [39]. However, this kind of comprehensive representation of the system constituents has not been
fully implemented in the simulation of SSN, since it requires co-simulation engines that are not available yet.

With the downscaling of MOSFET technology, circuits switch faster and a larger current variations \(\frac{di}{dt}\) are generated. Thus, SSN has become a critical issue in modern electronic system designs, even without considering the effect of the physical parallel-plate structure of the PDN. It should be pointed out that as \(\frac{di}{dt}\) increases, the coupling to parallel-plate modes also become stronger [42].

From Equation 2.17, it can be seen that a larger effective inductance or a higher rate of current change renders larger voltage fluctuations. Since the rate of current change depends on the system specifications, reducing the effective inductance in the power distribution network is a practical solution in decreasing the \(V_{SSN}\). In chapter 1, other methods for suppressing of SSN were presented. It was mentioned that a common approach to achieve this is by adding decoupling capacitors. The physical equivalent circuit for a decoupling capacitor is a series \(RLC\) resonance circuit [43]. This resonant circuit provide a shorting path for the noise. Noise filtering using this method is not very effective and omnidirectional stopband filters should be used to suppress the noise. A preliminary step in designing such filters is to know what the noise bandwidth is.
2.2.1 Frequency Spectrum of SSN

The common way to determine the SSN spectrum is by identifying the spectrum of the switching current. Consider the switching triggered by the transition edge of a clock signal thus having the same fundamental frequency. The waveform of the clock signal is represented by a periodic train of trapezoidal pulses as shown in Figure 2–8. Each pulse is described by amplitude $A$, pulse rise time $\tau_r$, fall time $\tau_f$, and pulse width $\tau$ [44].

![Figure 2–8: The periodic, trapezoidal pulse train representing clock signals of digital systems.](image-url)

From the SSN model defined in Equation 2.17, the waveform of SSN driven by the clock signal shown in Figure 2–8 is found to be another periodic pulse train as depicted in Figure 2–9. Note here that the noise waveform for only one switching device is shown. The pulse duration of the switching noise is primarily determined by the rise time and fall time of the clock.
If the pulse risetime equals the fall time, $\tau_r = \tau_f$, the Fourier series coefficients of the original trapezoidal waveform can be placed in a useful form as the product of two $(\sin x)/x$ terms:

$$c_n = A \frac{\tau}{T} \sin \left( \frac{1}{2} n \omega_0 \tau \right) \sin \left( \frac{1}{2} n \omega_0 \tau_r \right) e^{-jn\omega_0(\tau+\tau_r)/2} \quad (\tau_r = \tau_f) \quad (2.18)$$

Although the spectral components of periodic waveforms only exist at frequency $f = n/T$ for $n = 0, 1, 2, \ldots$, it is desirable to extract more intuitive information by generating the envelop of the spectral components, i.e., the upper bounds on the magnitude spectrum. The continuous envelop of the spectral components in the logarithmic scale can be obtained by substituting $f = n/T$ gives [44]:

$$20\log_{10}(\text{envelop}) = 20\log_{10}(2A\frac{\tau}{T}) + 20\log_{10} \left| \frac{\sin(\pi \tau f)}{\pi \tau f} \right| + 20\log_{10} \left| \frac{\sin(\pi \tau_r f)}{\pi \tau_r f} \right| \quad (2.19)$$
This shows that the composite plot is the sum of three plots:

\[
plot1 = 20\log_{10}(2A\frac{\tau}{T}) \quad (2.20)
\]

\[
plot2 = 20\log_{10}\left|\frac{\sin(\pi\tau f)}{\pi\tau f}\right| \quad (2.21)
\]

\[
plot3 = 20\log_{10}\left|\frac{\sin(\pi\tau_r f)}{\pi\tau_r f}\right| \quad (2.22)
\]

The composite plot shown in Figure 2–10 represents the bounds on the magnitude spectrum of a trapezoidal pulse train, which consists of three straight-line segments due to the asymptotes of the three plots above in Equation 2.22. The first segment is due to plot 1 and has a slope of 0 dB/decade. The second segment begins at \(1/\pi\tau\) and has a slope of -20 dB/decade. The third segment begins at \(1/\pi\tau_r\) and has a slope of -40 dB/decade.

\[\text{Figure 2–10: Bounds of the magnitude spectrum of a trapezoidal pulse train.}\]
If a trapezoidal pulse train with zero rise/fall time, \( \tau_r = \tau_f = 0 \), it gives a square wave as shown in Figure 2–11. The expansion coefficients of the square waveform would be

\[
c_n = A \frac{T}{T} \frac{\sin \left( \frac{\pi \omega_0 \tau}{2} \right)}{n \omega_0 \tau} e^{-j \omega_0 \tau / 2} \quad (\tau_r = \tau_f = 0)
\] (2.23)

![Figure 2–11: The square wave pulse train](image)

By applying similar analysis as for the trapezoidal waveform, the spectra envelop of the square wave is given in Equation 2.24 and plotted with bounds on the magnitude spectrum as shown in Figure 2–12.

\[
Envelop = A \frac{T}{T} \left| \frac{\sin (\pi \tau f)}{\pi \tau f} \right|
\] (2.24)

By comparing the spectra bounds of the trapezoidal waveform and square wave, it can be observed that the high frequency spectrum limit of the trapezoidal waveform is due to both the rise/fall time and the duration of the clock signal. The fast clock rate and transition time result in a wider noise spectrum with significant
Figure 2–12: Bounds on the magnitude spectrum of a square wave train.

spectral content at high frequencies.

Note that the clock signal and its derivative surge current are deterministic variables; however, data containing bit sequences of information in a digital system is obviously a random variable, whose behaviour can only be described statistically. An example of a random signal is pulse code modulation - non-return to zero (PCM-NRZ) waveform, as shown in Figure 2–13. A PCM-NRZ waveform assumes two binary states, 0 and 1 and may not require to return to zero in between each state transition [44]. A waveform that transitions between 0 and $X_0$ can be described as

$$x(t) = \frac{1}{2}X_0[1 + m(t)]$$  \hspace{1cm} (2.25)

where $m(t)$ is a random variable that assumes values of ±1 with equal probability in the bit interval of $nT < t < (n + 1)T$. 

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The autocorrelation function $R_x(\tau)$ of a random signal $x(t)$ is defined as the expected value of the product of the signal and the signal shifted in time by $\tau$:

$$R_x(\tau) = \overline{x(t)x(t+\tau)} \quad (2.26)$$

where the overbar indicates the statistical average of all possibilities [45].

In frequency domain, characterization of a random signal is in terms of its power spectral density (PSD), which is given by the Fourier transform of the autocorrelation function of the signal [44]:

$$G_x(f) = \int_{-\infty}^{+\infty} R_x(\tau)e^{-j\omega\tau}d\tau \quad W/Hz = \frac{X_0^2}{4}\delta(f) + \frac{X_0^2T}{4}\frac{\sin^2(\pi fT)}{(\pi fT)^2} \quad W/Hz \quad (2.27)$$

where $\delta(f)$ is the unit impulse function, it represents the value zero everywhere except at $x = 0$. 

Figure 2–13: A typical waveform of a PCM-NRZ signal.
From the PSD expression of PCM-NRZ waveform, it can be noticed that the second part of this expression, \( \frac{X_0^2 T \sin^2(\pi f T)}{(\pi f T)^2} \), is very similar to the square of the envelop expression for a square wave in Equation 2.24 by replacing \( A, \tau \) in the square wave with \( X_0, T \), respectively. Since the envelop is expressed by magnitude, which is the root of power as in the PSD expression. This indicates that the bandwidth found from the Fourier Series of a periodic clock signal can also be applied to determine spectrum of the pertinent digital data triggered by that clock.

### 2.3 Electromagnetic Bandgap (EBG) Structure

After determining the noise spectrum and considering a noise bandwidth, a 2-D distributed filter should be designed to enable the omni-directional suppression of the noise in the parallel-plate PDN. For this purpose, electromagnetic bandgap (EBG) structure was proposed which can offer a wideband and global noise suppression[3, 12]. The EBG structures in this application are composed of 2-D periodic metallic patterns. To suppress the noise, these geometries act like a high impedance surface (HIS) preventing wave propagation in a certain frequency range. This frequency range is referred to as the stopband of the EBG structure. It is determined by the geometry of each periodic unit cell and the dielectric characteristic of the substrate. The EBG structure shown in Figure 2–14 was first introduced by Sievenpiper for antenna applications to block the surface current and thus enhance the radiation efficiency [14]. Later, this concept was applied to suppress power/ground noise in power distribution network by replacing one of the power/ground planes with the EBG structure [3, 12]. This technique has proven to be able to extend the noise
suppression frequency range to a few GHz, instead of several hundred MHz that is achieved by using decoupling capacitors.

Figure 2–14: Top view and side view of mushroom-type EBG structure.

Mushroom-type EBG structure reported in [3, 12] (Figure 2–14), consists of square patterns connected to bottom solid plane with vias. This EBG structure has proven to be easily incorporated in commercial multilayer printed circuit board stack-ups, and provides an economic solution for suppressing power/ground noise.

Another type of EBG structure developed after the mushroom-type EBG does not contain vias and is referred to as the planar or uni-planar EBG structure [46]. One example of this type of EBG structure is shown in Figure 2–15. It contain two metal layers; one has a DC connected 2-D periodic pattern in order to be used as a reference voltage plane, and the other one is a solid conductor plane often used as ground. This structure is more attractive in terms of fabrication costs due to the elimination of vias. However, it has a major drawback, which is its susceptibility
to electromagnetic leakage and interference problems due to its patterned layer. In addition, the patterned surface can radiate. When a ground plane is placed on top to shield these radiations, it is shown that it can excite additional modes that can adversely impact the bandgap [47].

![Top View Side View](image)

Figure 2–15: Top view and side view of AI-EBG structure.

2.3.1 Analysis of the EBG-PDN

The bandgap characteristic of the EBG structures can be obtained from two methods. In the first method, the dispersion characteristics are predicted from Eigen-mode solutions, and plotting the dispersion diagram reveal the bandgap. Numerical solver and analytical solutions can be used to calculate the eigenvalues. Plotting the dispersion diagrams has been discussed in various contexts from solid state devices [48] to microwave periodic structures [49]. For this case, from the physical structure of a periodic lattice, a unit cell is identified and from there, a region or zone capturing all the possible non-repeating directions of propagation is found. This region is known as the irreducible Brillouin Zone [50]. To plot the dispersion diagram for
an EBG structure, the propagation constants of the propagating modes over the frequency range of simulation in all azimuthal directions of the 2-D periodic structure, as determined by the irreducible Brillouin Zone, are calculated. The frequency bands at which no real value for the propagation constant exist are the omni-directional bandgap of the EBG structure. Note that in this analysis, only the unit cell of the EBG structure is considered and simulated. However, the second method to find the bandgap focuses on the finite size structure. In this method, first two ports (or more) are defined on the finite size EBG structure. The insertion loss (or the $S_{21}$ plot between the ports) shows the stopband in the direction connecting the two ports. In addition to $S_{21}$, the other parameter that can be plotted is the transfer impedance ($Z_{21}$) between the defined ports.

In this thesis, a mushroom-type EBG structure which is a 2-D periodic structure as shown in Figure 2–16 is considered and its bandgap is found by using full-wave solver from the two methods described herein. The unit cell of this EBG structure, which is symmetric with respect to both x and y axis, is a square. The EBG structure is shielded as shown and has the geometrical parameters of $a = 10$ mm, $H = 0.508$ mm, $p = 9.6$ mm, $r = 0.2$ mm, $g = 0.4$ mm). In this design, the covered EBG structure is developed with three metal layers in the Rogers 4350B dielectric ($\epsilon_r = 3.48$, $\tan\delta = 0.003$).
Figure 2–16: Top view of the mushroom-type EBG surface with the side view of the covered structure. Note the design parameters and the unit cell are marked on the diagrams.

To simulate the dispersion diagram using a full-wave solver like Ansoft HFSS, periodic boundary conditions are applied to the four sides of the cell as shown in Figure 2–17. The periodic boundary conditions emulate the extension of the geometry to infinity on the x-y plane. The top and bottom planes of the unit cell are assigned Perfect Electric Conductor (PEC) to represent the power/ground conductor layers in the design.

The resultant dispersion diagram from the eigenvalue simulation of the structure depicts the relationship between the modal wave numbers or propagation constants versus frequency as shown in Figure 2–18. The x-axis is divided into three regions, and each one represents directions that are identified from the irreducible Brillouin Zone shown in the inset of Figure 2–18. By varying propagation directions in these region, the \( k - \beta \) diagrams or dispersion plots for all possible propagation modes in the EBG structure are found. As a reference, the linear \( k - \beta \) plots for a TEM wave propagation in the medium are shown with dotted lines. While the \( k - \beta \) plots in
the first and third regions demonstrate that for an EBG structure, the relationship of wave number and frequency is no longer linear. The gap between the two propagation modes, e.g. mode 1 and mode 2, represents a region that does not support wave propagation. Hence, figure 2–18 show that the bandgap is from 2.73 to 4.31 GHz.

Next, the transfer characteristics of a finite EBG structure are evaluated by generating $Z_{21}$ (the transfer impedance) and $S_{21}$. In the context of power integrity, the transfer impedance defines the ratio between the induced voltage at a victim port and the injected current at a source port. Therefore, $Z_{21}$ should be very small in order to block distribution of power/ground noise. Figure 2–19 shows the finite size EBG-PDN under study, which is composed of 10 by 10 unit cells with the same unit cell design parameters shown in Figure 2–16. The two ports (source and victim) are located at (0 mm, 50 mm) and (50 mm, 100 mm), respectively, between the power
Figure 2–18: Dispersion diagram of the EBG structure shown in Figure 2–16.

and ground layer.

Shown in Figure 2–19 is the side view of a standard parallel-plate PDN with the same port locations as the studied shielded EBG structure. By using Ansoft SIwave, the $Z_{21}$ profiles of these test structures are generated in Figure 2–20. From $Z_{21}$ profile of the parallel plate waveguide, high impedance peaks can be observed throughout the simulated frequency range. These peaks are generated due to the cavity mode resonances. The transfer impedance of the EBG structure is highly reduced from approximately 2 GHz to 4 GHz. This reveals suppression of the cavity modes at this frequency region, thus providing improvement of port isolation and suppression of
As mentioned earlier, insertion loss ($S_{21}$) is another parameter to characterize the noise suppression performance of an EBG structure. $S_{21}$ is defined as the ratio of the received voltage at the victim port to the transmitted voltage from the source port. In fact, the S-parameter matrix can be transformed into a Z-parameter matrix, and vice versa using straightforward relations [34]. For a reciprocal network terminated to matching loads (50 Ω for standard measurement conditions), the magnitude of $Z_{21}$ can be expressed in terms $S_{21}$ from [34]:

$$Z_{21} = \frac{100S_{21}}{1 - S_{21}^2}$$  \hspace{1cm} (2.28)
Figure 2–20: $Z_{21}$ parameters of the parallel-plate waveguide and parallel-plate PDN with the mushroom-type EBG structure of Figure 2–16.

To reconfirm $Z_{21}$ results, the insertion loss profiles of the studied EBG structure are generated with Ansoft HFSS. In these simulations, to evaluate the omnidirectional stopband, a number of ports are considered as shown in Figure 2–21. The area of the structure is 100 mm by 100 mm, which consists of 10 by 10 unit cells. The design parameters are consistent with previous test vehicle in Figure 2–16. Port isolation at three different directions is probed. Each port is represented with a surface mounted connector model and a through via connecting the top solid plane to the bottom ground plane.
Simulation results of the transmission coefficients between different ports are depicted in Figure 2–22. It can be observed that the induced stopband in all directions are very similar. If the stopband is determined from the sharp roll off at the lower frequency end to the subsequent transition to the higher $S_{21}$ magnitude, for example when reaching an apparent peak, the stopband of 2.2 to 3.8 GHz can be determined from Figure 2–22 in all directions. The attenuation in the stopband for the diagonal direction is slightly larger than those of the horizontal and vertical directions, since in this direction the incident wave travels through a higher number of EBG cells compared to the other two directions.
Figure 2–22: Transmission coefficients of the EBG structure for different port locations.

2.3.2 Mushroom-Type EBG-PDN with Through Vias

One of the concerns of using mushroom-type EBG structure in the practical power distribution networks is its fabrication cost and complexity, since it requires a large number of buried vias and an additional dielectric layer. In order to reduce the fabrication costs, the buried vias in the mushroom-type EBG structure of Figure 2–19 can be replaced by metallized through vias. To prevent shorting the top solid conductor plane to the bottom ground plane, an extra anti-pad (or clearance) is needed on the top plane for each through via as shown in Figure 2–23. The radius of the anti-pad considered in this study is 0.2 mm. Hence, the simulations conducted in Section 2.4.1 for the buried via structure are now repeated for the through via
configuration.

Figure 2–23: Simulation model to generate dispersion diagram of the EBG-PDN structure with through vias.

First, the dispersion diagram of the EBG unit cell with through via is extracted by Ansoft HFSS eigenmode solver as shown in Figure 2–24. It can be observed that the bandgap of the through via mushroom-EBG is from 2.76 to 4.39 GHz. Therefore, by comparing it to the the bandgap of the buried via structure in Figure 2–18, it can be concluded that the impact of using through vias is minimal.

Second, the port isolation performance of the through via EBG structure is verified with insertion loss simulations using Ansoft HFSS as shown in Figure 2–25. It should be pointed out that same port locations as shown in Figure 2–21 are considered in these simulations. By comparing the transmission coefficients shown in Figures 2–22 and 2–25, it is confirmed that the bandgap region remains the same.
when through vias are used. Therefore, the through via EBG structure has been proven to be an economical solution for practical implementations.

2.4 Summary

In this chapter, an overview of the most common type of power delivery networks consisting of a pair of power and ground planes in a parallel-plate arrangement is presented. Methods for analysis of this type of PDN are described followed by a discussion about signal routing within the PDN. Then, power/ground noise and simultaneous switching noise are introduced. EBG structures are also reviewed as they offer wideband noise suppression for modern PDNs that support today’s ever-increasing switching rates. One of the popular types of the EBG structures, which
Figure 2–25: Insertion loss profiles of the EBG structure with through vias at different directions.

is the mushroom-type EBG structure, is studied in this chapter. Its application for noise suppression is verified through simulations of S-parameters and generation of the dispersion diagram using a full-wave eigenmode solver. An example of an EBG structure embedded in a parallel-plate PDN, i.e. an EBG-PDN, is investigated and simulated in this chapter. It is shown that practical implementation of this EBG-PDN requires usage of through vias due to fabrication cost concerns. The simulations presented herein prove that the impact of such geometrical modifications is minimal on the bandgap which is the main noise suppression characteristics.
CHAPTER 3
Signal Integrity in Transmission Lines embedded in EBG-PDNs

Modern electronic circuits carry a much larger number of interconnects compared to their predecessors. Using high density interconnect (HDI) technologies in the design of electronics systems inevitably demands routing of signal lines within the PDNs. The newly emerged EBG-PDN solution should also accommodate a large number of signal lines. This result in routing the lines above or maybe within the EBG structure. The signal integrity of such lines is prone to be degraded considerably due to the discontinuities in the return current path as the lines are referenced to the EBG surface.

In this chapter, the impact on signal integrity of interconnects backed by a mushroom-type EBG structure is investigated. First, four trace routing scenarios are introduced. Then, the signal integrity is evaluated for each scenario through full-wave simulations. A prototype based on one of the routing cases is fabricated, and measured to observe the insertion loss and output eye diagrams in the time domain.
3.1 Signal Line Routing Scenarios

When an EBG structure is incorporated in a parallel-plate PDN, it is embedded into a multi-layer stackup in the same way as an embedded decoupling capacitor is realized as shown in Figure 3–1 (a). In an embedded decoupling capacitor, a high-k thin film layer is buried in the substrate, which prohibits signal lines to be routed within this layer. While for an EBG structure (Figure 3–1(b)), it is possible to use a regular lower permittivity material. Therefore, it is feasible to route signal lines within EBG structure layers. This allows for further utilization of the substrate volume, and accommodating for a higher density of interconnects.

![Embedded Decoupling Capacitor](a) ![Mushroom-type EBG structure](b)

Figure 3–1: (a) An embedded decoupling capacitor, (b) A mushroom-type EBG structure in a PDN.

Four possible scenarios are considered in this thesis for routing a single ended trace in a mushroom EBG-PDN. These are depicted in Figure 3–2 and described as follows:

- **Case A:** The signal line is routed above a row of buried-vias in a mushroom EBG-PDN with buried vias.
Figure 3–2: Possible signal line routing scenarios in EBG-PDN.

- **Case B**: The signal line is routed above the gaps between the patches in a mushroom EBG-PDN with buried vias.
- **Case C**: The signal line is embedded within the EBG substrate underneath the gap between the patches in a mushroom EBG-PDN with buried vias.
- **Case D**: The signal line is routed above the gaps, between the patches in a mushroom EBG-PDN with through via.

For all studied cases in this thesis, the single ended trace is designed to be placed at the mid-height of a 0.508 mm thick Rogers 4350B substrate. The width of the line is 0.24 mm and the conductor thickness is 0.0017 mm to obtain a 50 Ω characteristic impedance when a symmetric stripline is considered as shown in Figure 3–3.

As seen from Figure 3–2, in all cases, the EBG surface is one of the return current paths for the signal. From the signal integrity point of view, when the return
current comes across a discontinuity such as a split or a via, it is displaced and some of the transmission energy is scattered into unwanted modes. These discontinuities also reflect the signal back to the source, or towards the edges of the substrate and result in unwanted radiation, conducted emissions, and electromagnetic interference problems.

3.2 Characterization Through Full-wave Simulation

3.2.1 Simulation Set-up

To evaluate the signal integrity in the described case studies, full-wave simulations are conducted. The main parameter to observe is the insertion loss. It is best if 3-D full-wave solver are used as opposed to 2-D solvers due to the presence of vias. Setting proper simulation boundaries and port definitions is critical for generating reliable results, especially in conducting Ansoft HFSS simulations.

In HFSS, there are two ways to define the ports: lumped port and wave port [51]. Lumped ports are recommended for cases where the excitation source is located internal to the geometric model, while wave ports are defined on a surface boundary. For lumped ports, the excitation on lumped source is applied brute force between two
conductor edges. As a result, parasitic field components in the vicinity of a lumped port are introduced due to the discontinuity in the port junction. However, wave ports do not introduce the undesirable modes. Thus, in the simulations presented in this section, wave ports are preferred.

The width of a wave port should be assigned properly to ensure the correct calculation of the port impedance. Therefore, a proper width for the port should be considered, which is usually wider than the width of the transmission lines. In all of the studied cases, the width of the transmission line is 0.24 mm, and the distance between the line and reference plane is 0.508 mm, so that the width of the wave port is considered to be 2 mm as shown in Figure 3–4. All conductors in this simulation are set with finite conductor boundary to include all conductive losses. Also, the wave port needs to be symmetric with respect to the stripline and the reference planes to minimize discontinuities.

![Figure 3–4: Wave port definition for the stripline shown in Figure 3–3.](image)

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Figure 3–5 shows the $S_{21}$ of the stripline configuration shown in Figure 3–3 using the symmetric wave ports at its two ends. It can be observed that the stripline impedance is almost well-matched to 50 Ω up to 10 GHz, and the insertion loss profile is resonance free. This confirms the correct definition of the wave ports.

Figure 3–5: Insertion loss profile for the stripline in Figure 3–3.

Another factor which should be taken into consideration in the simulations is the definition of the boundary surfaces. In the studied cases, strong cavity modes might be excited due to the splits on the EBG surface. If open boundary condition is applied to the side faces of the geometry, the excited mode would bounce back and forth in the structure, resulting in multiple resonance dips in the insertion loss profile. Therefore, radiation boundaries should be applied to the side walls. In this
situation, the scattered energy is absorbed by the boundary and prevented from being further reflected.

Figure 3–6 shows the $S_{21}$ parameter for Case A with open and radiation boundary conditions. It can be seen that in the case of open boundary, there are multiple deep resonances around 2 GHz, while for the radiation boundary case, only one resonance dip is found around 2 GHz.

![Figure 3-6: Magnitude of $S_{21}$ for Case A with open and radiation boundaries.](image)

3.2.2 Full-wave Simulation Results of the Four Cases

The transmission coefficients of the four cases depicted in Figure 3–2 are obtained by using Ansoft HFSS solver with the radiation boundaries and symmetric wave port configurations. In all cases, the length of the transmission line is 100 mm and a 10 by 10 cell mushroom EBG structure as described in Section 2.3 and Figure...
2–19. Note that the area of the structure is 100 mm by 100 mm.

As depicted in Figure 3–7, the signal transmission of all studied cases is degraded considerably compared to that of the benchmark regular stripline. Three main resonance dips marked as \( f_1, f_2 \) and \( f_3 \) are observed in the \( S_{21} \) of Cases A, B, C and D in the figure, which are around 2.2 GHz, 3.8 GHz, and 8 GHz, respectively. Distinct differences between Case A and the other three cases are noticed; first, when the signal line is not routed above the gaps, for example, in Case A, the insertion loss has a deeper low resonance dip around \( f_1 \), while showing a much better performance at the high frequency region (note the dip at \( f_3 \)), compared to the other cases where the signal line is routed above the gap between the rows of EBG cells. It should be reminded that from dispersion diagram simulations of Chapter 2, it is known that the bandgap induced by the EBG structure is between 2.1 - 3.8 GHz for the buried via, and between 2.2 - 3.8 GHz for the through via EBG structures.

3.2.3 Inspection of the Insertion Loss Profiles

By comparing the insertion loss profile for case D with that of Case A, a noticeable difference in the location of the first resonance dip is observed. Note that the first dip for Cases A, B, and C are around \( f_1 \) while for Case D it is around \( f_2 \). It can be concluded that as the buried via is replaced by through via in the EBG-PDN, the first resonance dip in the insertion loss shifts to a higher frequency, while the dispersion simulations in chapter 2 show a minimal impact on the bandgap. Therefore, it is determined that the influence resulting from the modification in the geometry is
Figure 3–7: Simulated magnitude of $S_{21}$ for all of the studied cases shown in Figure 3–2 and Figure 3–3.

stronger on the signal integrity rather than the power integrity. It can be speculated that the location of the first resonance dip depends on the height of the via in the EBG structure.

In order to investigate the origin of the high resonance dip ($f_3$), which is pretty much co-located for all cases, a test is conducted by removing the via in the EBG structure as shown in Figure 3–8. In this test, the signal line is placed as Case B except that all the vias are removed and only EBG patches exist.

Figure 3–9 presents the comparison of the transmission coefficients of Case B and the structure of Figure 3–8. It can be clearly observed that the low resonance
Figure 3–8: The test configuration in which the signal line is routed above the gap between the EBG patches and the vias are removed.

dip \( (f_1) \) disappears in the insertion loss profile of the test structure without vias, but the high resonance dip \( (f_3) \) remains almost the same. This result confirms the earlier conclusion. It can be speculated that the first resonance dip is associated with the vias of the EBG structure, and the second frequency dip is related to the gap between the EBG patches.

Figure 3–9: Simulated \( S_{21} \) of Case B and test structure shown in Figure 3–8.

3.3 Observation of the Return Current Path

When the signal current is launched on the transmission line, it propagates along the line and needs to flow back to the source through the return path in order to
complete the current loop [8]. In packages and PCBs, the return current flows on the reference plane in close proximity to the signal line as shown in Figure 3–10. This is because the return current always flows in the path of the least inductance by means of minimizing the total current loop area [52].

![Diagram](image)

Figure 3–10: signal current loop through the transmission line and back on reference plane.

In a stripline configuration, since the trace is sandwiched between two reference planes, the return current has two routes back to the source. The proportion of the current flowing in each return path depends on the closeness of the trace to each plane [53]. Therefore, for the symmetric stripline shown in Figure 3–3, the return currents on each plane are identical. This is confirmed by the surface current density plots on both reference planes from Ansoft HFSS. As shown in Figure 3–11, the return current on both planes is confined in the area which is upward or downward projection of the signal trace.
Figure 3–11: Magnitude of the surface current density $J_{vol}$ on both (a) top and (b) bottom reference planes at 3 GHz.
If anything disturbs the current loop, the signal integrity is compromised [8]. For example, when the return current sees a gap discontinuity, its return path is disrupted since no conducting path is provided between the two planes separated by the gap. Hence, the polarization charges are created on the two patches in order to balance the charge distribution [20]. Also, part of the return current could be forced to detour along the edges of the patch. In this situation, the return current loop area is increased, resulting in further transmission delays and potential crosstalk when other interconnects are present. Therefore, it helps to understand the signal integrity problems by examining the return current on the reference planes.

The return current paths are disrupted for all routing cases as shown in Figure 3–2. In Case A, a row of mushroom-type EBG cells are placed just underneath the signal line, therefore, the return current path is inevitably disturbed by the gaps between the adjacent patches. Figure 3–12 plots the magnitude of the surface current density on the EBG surface just underneath the signal line for Case A at 3 GHz, 6 GHz and 8 GHz, respectively. These three frequencies are chosen since 3 GHz is within the stopband of the mushroom-type EBG structure, 6 GHz is outside of the stopband, and 8 GHz is the resonance frequency at $f_3$. 
Figure 3–12: Case A: Magnitude of the surface current density $J_{vol}$ on the EBG surface underneath the signal line at (a) 3 GHz (within the bandgap), (b) 6 GHz (outside of the bandgap, (c) 8 GHz ($f_3$).
As shown in Figure 3–12 (a), the return current, which crosses over the splits on the EBG surface, is concentrated underneath the signal line at 3 GHz. The frequency is within the bandgap of the EBG structure, which means that the EBG bandgap prevents the distribution of the current across the EBG surface. As frequency increases beyond the bandgap region, part of the return current detour toward the edge of the patches (3–12 (b) and (c)).

For Cases B, C and D in Figure 3–2, the signal line is routed above the gaps between two rows of EBG cells. In this situation, the signal line is not only routed in proximity of EBG cells, but also the area on the EBG surface just underneath the signal line is void, which greatly complicates the return current paths on the EBG surface plane. Figure 3–13 presents the distribution of the return current on the EBG surface for Case B to represent all the three cases at 3 GHz, 6 GHz and 8 GHz, respectively.

It can be seen from Figure 3–13 that the return current are mostly concentrated underneath the signal line on the edges of two rows of EBG cells, which is quite similar to that of Case A. However, the situation is greatly worsened at 8 GHz, which is the resonance dip $f_3$ in the insertion loss profile shown in Figure 3–7. At this frequency, the return current is coupled to several rows of EBG cells and almost spread over the entire EBG surface, which exhibits higher potential for creating EMI problems.
Figure 3–13: Case B: Magnitude of the surface current density ($J_{vol}$) on the EBG surface underneath the signal line at (a) 3 GHz (within the bandgap), (b) 6 GHz (outside of the bandgap), (c) 8 GHz ($f_3$).
3.4 Fabricated Prototype and Measurements

3.4.1 Fabricated Prototype Case D Interconnect

A test board based on Case D structure is prototyped to observe signal transmission in the interconnect loaded with the EBG structure. The board has the area of 80 mm by 60 mm containing an 8 by 6 array of through via EBG unit cells. Due to the limitation of the fabrication area, 10 by 10 array was not possible. Rogers 4350B substrate was used for fabrication. The geometrical parameters of the unit cell are the same as the simulated structure ($a = 10 \text{ mm}$, $H = 0.508 \text{ mm}$, $p = 9.6 \text{ mm}$, $r = 0.2 \text{ mm}$, $g = 0.4 \text{ mm}$). Two plated through hole vias are placed at (10 mm, 30 mm) and (70 mm, 30 mm) for connecting the vertical mount SMA connectors and feeding the transmission line, as shown in Figure 3–14. The length of the signal line between the two ports is 60 mm. Figure 3–15 shows the photo of the fabricated prototype. The outer conductor of the two vertically mounted SMA connectors are soldered to the top conductor plane.

![Figure 3–14: Side view illustration of case D test board](image-url)
3.4.2 S-parameter Measurement

The S-parameters of the test board were measured by an Anritsu 37397D Vector Network Analyzer from 1 MHz to 10 GHz. In order to verify the results, Ansoft HFSS was used to simulate the S-parameter of the test structure. In the simulation, the port definition is simplified by using waveports at both ends of the signal line, and the model of the SMA connectors is not included. Figure 3–16 shows the measurement and full-wave simulation results showing very good correlation. The two prominent transmission dips observed earlier for Case D structure with larger size board are also present in both simulated and measured insertion loss profiles here.

3.4.3 Eye Diagram Measurement

Often signal integrity of the interconnects is characterized in the time domain by observing ringing, delay, distortion and reflection. A common method used to evaluate these parameters is through eye diagram measurements by identifying the eye opening of the output eye pattern. A larger eye opening is desirable for practical application in order to avoid detection errors. Parameters, such as peak-to-peak
Figure 3–16: Measured and Simulated $S_{21}$ of case D test structure.

voltage, eye height, eye width, and jitter are often inspected to determine the eye quality [54].

Using the test set-up shown in Figure 3–17, a stream of pseudo-random binary sequence (PRBS) pulses with fixed rise/fall time of 60ps was produced by an Anritsu MP1763 pulse pattern generator. The pulse pattern generator itself was triggered by an RF signal generator which was an Anritsu MG3692A CW generator. The data rate can be changed by tuning the frequency of the RF signal generator. The eye diagrams were generated at the data rates of 3Gb/s, 5Gb/s and 7Gb/s. The generated pulses have a magnitude of 1.0 V, so the ideal magnitude of the output of DUT is 0.5 V since the voltage is divided between the characteristic impedance of
the cables and the internal resistance of the pattern generator.

![Diagram](image)

Figure 3–17: Eye diagram measurement set-up.

The measured eye diagrams are presented in Figure 3–18. As well, in Table 3–1, the measured eye-diagram parameters are summarized. In the table, the $V_{p-p}$ is the voltage measured at the outer edges of the output eye pattern. Ideally, the output $V_{p-p}$ would be 0.5 V, but larger $V_{p-p}$ is observed due to the non-ideal behaviors introduced by the test structure and measurement system. Eye height dictates the amount of noise margin that the system can tolerate. In our analysis, the eye height is measured as the minimum eye opening within the 20% span of the eye width around the center of the eye, as indicated in Figure 3–18. Eye width is the time interval over which the waveform can be uniformly sampled without decision errors. Finally, jitter is the time-base variation of the pulse from its ideal location, which causes a reduction in the optimum sampling time. The ideal location can be defined as the
delayed version of the input signal ignoring any system imperfections. In this thesis, peak-to-peak jitter is measured at the threshold crossing, i.e., half of the eye height. In common practice, an eye mask, which is specific to a signalling standard, is used to assess the overall quality of an eye pattern [54]. As can be seen, the performance of the Case D interconnect deteriorates rather rapidly as the data rate increases. For example, when the data rate is 5 Gb/s, the eye height is about half of the source voltage magnitude, while when the data rate is 7 Gb/s, the eye height is less than 1/3 of the source voltage magnitude. This in time domain manifests as closing of the eye.

Table 3–1: Parameters of fabricated prototype based on case D

<table>
<thead>
<tr>
<th>data rates</th>
<th>3 Gb/s</th>
<th>5 Gb/s</th>
<th>7 Gb/s</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{p-p}$ (mV)</td>
<td>602.50</td>
<td>680.00</td>
<td>830.00</td>
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<td>146.94</td>
</tr>
<tr>
<td>Eye Width (ps)</td>
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<tr>
<td>Pk-Pk Jitter (ps)</td>
<td>18.00</td>
<td>33.60</td>
<td>64.50</td>
</tr>
</tbody>
</table>
Figure 3–18: Eye diagram measurement results of Case D test structure at the data rates of 3, 5 and 7 Gb/s.
3.5 Summary

The quality of signal transmission in single ended traces routed in an EBG-PDN is evaluated in this chapter. Four scenarios of routing possibilities are considered when an EBG-PDN is used. The insertion loss profiles of the four cases are generated by a 3-D full-wave solver (Ansoft HFSS). The simulation results show that the signal transmission quality is degraded considerably in these four cases, since the EBG structure introduces discontinuities in the return current path. Also, by examining the surface current on the EBG surface, it can be observed that the interruption of the return current path causes potentially EMI problems. A test structure is fabricated and experimentally evaluated in both frequency and time domain. Measurements of $S_{21}$ and eye diagrams demonstrate reduction of the transmission coefficient and generation of sharp transmission dips, as well as closing of the eye, especially at high data rates.
CHAPTER 4
Modeling of Signal Lines Backed by a Mushroom-type EBG Structure

This chapter describes the modelling and analysis of the signal line routed in a mushroom-type EBG-PDN. The mushroom-type EBG-PDN was introduced in Chapter 2 and demonstrated excellent noise suppression characteristics. However, when single-ended traces are routed in this EBG-PDN, the signal integrity is degraded considerably. This was analyzed through full-wave simulations and measurements in Chapter 3. In this chapter, a modelling methodology based on using static lumped circuits for the mushroom-type EBG structure is proposed. The developed model is integrated with the transmission line in order to conduct global circuit simulations. S-parameter simulations are performed to validate the model with full-wave simulations.

4.1 Development of the Equivalent Circuit

4.1.1 Return Current Paths

As discussed in Chapter 3, when a single ended trace is embedded within a mushroom-type EBG-PDN, several resonance dips are observed in the insertion loss profile due to discontinuities introduced by the EBG structure in the return current paths. Also, it was found that the low resonance dip ($f_1$ for Case A, B and C; $f_2$ for
Case D) were related to the vias in the EBG structure, while the second resonance
dip was associated with the the gaps between EBG cells. The objective here is to
extract lumped models to capture these resonance dips. Although full-wave solvers
are used to obtain accurate results, lumped equivalent circuits are often preferred
at the initial and optimization design stages for fast and simple prediction of sys-
tems performance [55]. Therefore, an equivalent circuit, which can be incorporated
into traditional SPICE-type simulators to enable global simulations is highly desired.

As shown in Figure 4–1, it can be observed that three possible paths for the
return current can be identified. The first and uninterrupted return current path is
on the top solid conductor plane. The other two paths are formed through the EBG
structure: one is on the EBG patch surface and bridges across the gap between the
patches through fringing capacitances, and the other one flows through the EBG via
and the vertical capacitance coupling to the bottom solid conductor plane. There-
fore, the equivalent model for the signal line routed within an EBG-PDN should
reflect these possibilities of return current paths.

4.1.2 Development of the Equivalent Circuit for the EBG-PDN

The circuit model for a mushroom-type EBG unit cell with buried via is devel-
oped as shown in Figure 4–2. Note that signal line is not included here. The model
consists of three parts. The first part describes the characteristics of the EBG patch
plane; the capacitive coupling between two adjacent patches are shown by the capac-
itance $C_{\text{gap}}$, the inductive coupling between these patches are represented by $L_{\text{patch}}$. 

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Figure 4–1: Signal current and the return current paths of a transmission line routed within a mushroom-type EBG-PDN.

and the conductor losses of each patch is considered by $R_{\text{patch}}$. This resistance is small at low frequencies and can be ignored for common conductors used in PCBs. The second part of the model captures the coupling to the top conductor plane as shown by $C_{\text{patch}}$ between the patch and the top solid plane. The third part of the model represents the path for the current flow through the vias and to the bottom conductor plane, which includes the inductance of the via, $L_{\text{via}}$, and $C_{\text{patch}}$ showing the capacitance coupling between the patch and the bottom plane.

The equivalent circuit for a mushroom EBG-PDN with through vias is also developed in the same fashion, as shown in Figure 4–3. The only difference is the through via is extended to the top plate and an additional inductance, $L_{\text{via}}$, is added in parallel with the $C_{\text{patch}}$ between the patch and top solid plane. Since the spacing
between the patch and the top and bottom conductors planes are equal in this studied case, the parallel LC circuit representing sections above and below patches are the same.

Figure 4–3: The equivalent circuit for the unit cell of an mushroom-type EBG-PDN with a through via.
4.1.3 Determining the Values of the Equivalent Circuit Elements

In order to extract the value of an element in a model, three methods are often considered. The first method uses the simulated full-wave S-parameters of the structure and numerically fits the S-parameters of the model by using optimization function of a CAD solver like Agilent ADS. The extracted values from this method are accurate. However, the lengthy full-wave simulations are still needed, and the optimization process requires slowly converging procedures. The second approach is by using a quasi-static solver such as Ansoft Q3D extractor. This quasi-static technique assumes that there is no interaction between the electric and magnetic fields within the problem space, and hence, it reduces the number of equations to be solved and results in minimizing the calculation time [56]. The third approach is by using available closed-form formulas to find the values of circuit elements. This method is obviously fast, but in many cases approximations are made which trade off the accuracy. In this thesis, both quasi-static approach by Ansoft Q3D extractor and close-form formulas are used to extract the values of the circuit elements.

From the closed-form relation given in [14, 57], the gap coupling capacitance can be calculated from the following equation:

\[ C_{\text{gap}} = \frac{W \varepsilon_o \left( \varepsilon_{r1} + \varepsilon_{r2} \right)}{\pi} \cosh^{-1} \left( \frac{2W}{g} \right) \]  \hspace{1cm} (4.1)

where \( W \) is the width of the square patch, \( g \) is the spacing between the patches, and \( \varepsilon_{r1} \) and \( \varepsilon_{r2} \) are the permittivity of the material above and beneath the patches,
respectively.

Equation 4.2 determines the value of the inductor $L_{\text{via}}$ and is taken from [58].

$$L_{\text{via}} = \frac{\mu_0}{2\pi} d \left( \ln \left( \frac{2d}{r_v} \right) + 0.75 \right)$$

(4.2)

where $d$ is the height of the via, $r_v$ is the via radius and $\mu_0$ is the permeability of free space.

$C_{\text{patch}}$, which denotes the coupling between the patch and a solid conductor plane, is modelled as a parallel-plate capacitance without considering the fringing field effect at the edges, as given in Equation 4.3 from [8].

$$C_{\text{patch}} = \frac{\epsilon W}{d}$$

(4.3)

$L_{\text{patch}}$, which represents the inductive coupling between the adjacent patches is given in Equation 4.4, obtained from [34].

$$L_{\text{patch}} = \frac{\mu_0}{\pi} \cosh^{-1} \frac{t}{W}$$

(4.4)

where the $t$ is the thickness of the conductor, and it is 0.017mm for 0.5 oz copper.

$R_{\text{patch}}$, which accounts for the resistive losses of the patch, is given in Equation 4.5 by the resistance of a conductor with a uniform rectangular cross section.
\[ R_{\text{patch}} = \frac{\rho}{t} \]  

(4.5)

where \( \rho \) is the bulk resistivity of the conductor. The units of resistivity is \( 1/\Omega m \).

Consider the geometrical parameters of a mushroom-type EBG structure as shown in Figure 2–16. The values of the lumped circuit elements of the model are easily calculated by the closed-form formula mentioned above. These calculated values are validated using a quasi-static solver, i.e. Ansoft Q3D Extractor. A structure composed of 2 by 2 mushroom-type EBG cells with the same geometrical parameters was created in Q3D to calculate the capacitance and resistance values. The \( R_{\text{patch}} \) was found to be negligible (around 0.001 \( \Omega \)) for the patch with an area of 9.6 mm by 9.6 mm, as expected. The parallel-plate capacitance between each patch to the top or bottom conductor plane is 5.8 \( pF \), and the fringing capacitance between two adjacent patches was found to be 0.778 \( pF \). The partial inductance matrices were also extracted by specifying proper source and sink excitations. When the source and sink excitations were assigned on the patch and bottom conductor plane as shown in Figure 4–4 (a), the inductance between them was obtained as 0.38 \( nH \). This inductance value is close to 0.35 \( nH \), the inductance extracted from a via with the height of 0.508 mm and the diameter of 0.2 mm by applying source and sink on the top and bottom surface of the single via as shown Figure 4–4 (b). Therefore, it is considered that the partial inductance between the patch and bottom conductor plane in the circuit model can be approximated as the inductance of the via. The mutual inductance between adjacent patches is extracted as 1.2 \( nH \) by using the excitation
arrangement shown in Figure 4–5. Note the inductance between patches is divided into two elements ($L_{patch}$) of the value 0.6 $nH$ since a T model is issued ultimately. The results obtained from Q3D extractor are compared with those calculated using closed-form relations in Table 4–1, showing excellent accuracy of Equation 4.1 to 4.5.

Figure 4–4: The excitation configuration in Ansoft Q3D to extract (a) the inductance between the patch and bottom conductor plane. (b) the inductance of the via.

Figure 4–5: The excitation configuration in Ansoft Q3D to extract the mutual inductance adjacent patches.

4.1.4 Including the Transmission Line in the EBG-PDN Model

In the model developed in Section 4.1.2, the unit cell of the covered EBG structure is presented with an RLC circuit. The models given in Figure 4–2 for the patch surface, the via and lower conductor are considered in the form of the T network as
Table 4–1: Values of the circuit elements in the model of mushroom-EBG structure

<table>
<thead>
<tr>
<th>elements</th>
<th>closed-form formula</th>
<th>Q3D</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{patch}$ (Ω)</td>
<td>0.001</td>
<td>0.001</td>
</tr>
<tr>
<td>$L_{patch}$ (nH)</td>
<td>0.552</td>
<td>0.6</td>
</tr>
<tr>
<td>$C_{patch}$ (pF)</td>
<td>5.8228</td>
<td>5.8</td>
</tr>
<tr>
<td>$C_{gap}$ (pF)</td>
<td>0.72891</td>
<td>0.778</td>
</tr>
<tr>
<td>$L_{via}$ (nH)</td>
<td>0.35895</td>
<td>0.35</td>
</tr>
</tbody>
</table>

shown in Figure 4–6 (a). Due to the symmetry of the structure, $R_{patch}$ and $L_{patch}$ are divided by 2 in the two sides of the via. Note here that the capacitive coupling to the top plane is included by doubling $C_{patch}$ in parallel with $L_{via}$. When the entire EBG structure is considered, these RLC blocks representing the cells are periodically cascaded as shown in Figure 4–6 (b). In this manner, 1-D and 2-D equivalent circuit for the EBG-PDN can be created.

To capture the effect of the EBG structure on the signal transmission, the signal line should also be included in the model. A simple transmission line model as shown in Figure 4–7, or a distributed RLGC circuit representation of a transmission line as discussed in Chapter 2 can be integrated with the EBG-PDN model. The input source and terminating load at the end of the line are easily included in the model at the two ends of the signal line, as shown in Figure 4–7.
4.2 Simulations and Discussion of the Results

The modelling of the EBG-PDN can be developed either in one-dimentional or two-dimentional fashion by implementing the T-model of the unit cell with the 1-D or 2-D configuration, respectively. The 1-D model obviously requires less circuit elements to represent the EBG-PDN, so it can reduce the number of equations to be solved and thus save simulation time. However, since this 1-D model assumes that the return current is confined underneath the signal line, it can only be employed for Case A due to the return current analysis presented in Section 3.3. In order to represent Cases B, C and D, where the signal line is routed above the gap between two rows of EBG cells, a 2-D model is employed to account for fringing capacitance.
4.2.1 Signal Line in Case A

For evaluation of the model, first a 1-D equivalent circuit is used to approximate the EBG-PDN of Case A. The insertion loss between the two ends of the line in Figure 4–7 is simulated using the RLC values determined by the closed-form formulas as given in Table 4–1. Full-wave simulations using Ansoft HFSS are conducted for comparison as well.

As shown in Figure 4–8, a reasonable agreement between full-wave analysis and equivalent circuit simulation is achieved in the studied frequency band. The two resonance frequencies in the $S_{21}$ profile are accurately captured from circuit simulation. There are some discrepancy between the circuit model and full-wave simulations in predicting the insertion loss at the high frequency resonance of 8 GHz, which is due

Figure 4–7: Model for the signal line embedded in an EBG-PDN.
Figure 4–8: $S_{21}$ of Case A structure (shown in Figure 3–2) from full-wave and circuit simulations.

to the frequency-independent model used.

### 4.2.2 Signal Line in Case B, C, and D

The model is extended to include lines embedded in EBG-PDN for Cases B, C, and D. Since the signal line is routed above the gap between two rows of EBG cells in these situations and the return currents are not confined underneath the signal line, the 1-D equivalent circuit needs to be modified and cascaded in a 2-D fashion as shown in Figure 4–9. This circuit prototype is the same when the signal line is placed above or under the EBG surface plane. Therefore, the model for Cases B and C are the same. For Case D, another $L_{via}$ component needs to be added in parallel with $C_{patch}$, as shown in Figure 4–3, to account for the through via.
The $S_{21}$ results from circuit solutions are compared with Ansoft HFSS simulations in Figure 4–10 and Figure 4–11 for Cases B, C and D, respectively. A good prediction of $S_{21}$ is obtained for each simulated case using the proposed equivalent circuits.

### 4.2.3 Discussion of the Results

The results presented in Section 4.2.1 and 4.2.2 all capture the resonance dips in the insertion loss profiles ($f_1$ and $f_3$ for Cases A, B and C, $f_2$ and $f_3$ for Case D) as observed in Figure 3–7. The model reveals that the two resonance frequencies are due to resonances of two LC pairs. One pair is composed of $L_{patch}$ and $C_{gap}$, which forms the return current path on the EBG patch surface as mentioned before. The other resonance is due to $L_{via}$ and $C_{patch}$, which represent the return current path through the EBG vias and the parallel-plate capacitor between the patch and the
solid reference plane. Calculations of the resonance frequencies due to these LC pairs predict the dips in $S_{21}$ plot and show good agreement with full-wave simulations discussed in chapter 3 (from full-wave simulation, $f_1 = 2.2$ GHz, $f_2 = 3.8$ GHz and $f_3 = 8.0$ GHz).

Calculation of the resonance frequency $f_1$:

$$f_1 = \frac{1}{2\pi \sqrt{L_{via}C_{patch}}} = \frac{1}{2\pi \sqrt{0.35 \times 5.8 \times 0.35 \times 5.8}} = 2.6 \text{ GHz} \quad (4.6)$$

Calculation of the resonance frequency $f_2$:

$$f_2 = \frac{1}{2\pi \sqrt{2 \times L_{via}C_{patch}}} = \frac{1}{2\pi \sqrt{2 \times 0.35 \times 5.8 \times 0.35 \times 5.8}} = 3.7 \text{ GHz} \quad (4.7)$$
Figure 4–11: $S_{21}$ of Case D structure (shown in Figure 3–2) from full-wave and circuit simulations.

Calculation of the resonance frequency $f_3$:

$$f_3 = \frac{1}{2\pi \sqrt{L_{\text{patch}} C_{\text{gap}}}} = \frac{1}{2\pi \sqrt{0.54 nH \times 0.73 pF}} = 7.9 \text{ GHz}$$

where values of $L_{\text{via}}$, $C_{\text{patch}}$, $L_{\text{patch}}$ and $C_{\text{gap}}$ are given in Table. 4–1.

The formulas show that the S-parameters of the signal lines routed in an EBG-PDN are dependent on the design parameters of the EBG structure. Therefore, by varying the physical parameters that are modelled by the two LC pairs, the resonance frequencies can be tuned. For example, in order to move $f_1$ to an upper frequency, we can either reduce via inductance, which can be done by increasing the via diameter, or increasing its height. As a result, the signal integrity degradation can be
alleviated at the lower frequency region. The same discussion can be employed to avoid the $f_2$ and $f_3$ resonance dips.

4.3 Summary

In this chapter, first, the equivalent circuits for the unit cell of a mushroom-type EBG-PDN structure with both buried vias and through vias are introduced. The value of the circuit components of the model is extracted by using closed-form formulas, which are also verified with a quasi-static solver. The unit cell model are cascaded in 1-D or 2-D fashion to represent the EBG-PDN. To capture the possible routing scenarios discussed in chapter 3, a transmission line model is included in the EBG-PDN equivalent circuit. Therefore, fast circuit simulation are enabled by using the developed models. The results from the circuit simulation are compared with full-wave analysis which show a very good agreement for all the studied cases. The models provide insight into the factors affecting the signal integrity in these embedded interconnects, and allow for calculation of the dips in the $S_{21}$ plots by using simple LC resonance equations.
CHAPTER 5
Modifying the EBG Structure by Insertion a Conductor Island

As discussed in Chapters 3 and 4, the signal integrity of a signal line routed in an EBG-PDN is impaired due to the discontinuities in the return current path. The increase of the operating frequency also worsens this problem. Therefore, in order to improve the signal integrity and maintain the noise suppression characteristics of the EBG, the PDN structure should be modified. In this chapter, a conductor island is inserted on the EBG surface and placed underneath the signal line. This island provides an uninterrupted return path for the signal while maintaining the noise suppression feature of the EBG-PDN. It will be shown in this chapter that the signal line backed by the island in the EBG demonstrates similar transmission quality as that of a regular stripline.

5.1 Design of the Conductor Island in the EBG Structure

The fields of a stripline interconnect is mainly concentrated between the signal strip and the top, and between that and the bottom conductors. The return current on the planes also flow in a narrow paths which are approximately the projections of the strip on the top and bottom planes. From this fact, it can be concluded that in a EBG-PDN structure, if a narrow solid strip is inserted underneath the signal
strip, the signal integrity problems will be diminished. This conductor strip looks like an island surrounded by EBG cells on its two lateral sides. The strip should be connected to the bottom ground plane as shown in Figure 5–1.

Figure 5–1: Top and side views of a signal line routed above a solid conductor island in the EBG structure (case E).

The three parameters in the design of the island strip are: its width, the location and the number of the grounding vias. Ideally, the width of the island should be as small as possible to maintain the noise suppression of the EBG structure. The number of vias should be kept as few as possible to avoid additional fabrication cost and complexity. It is found from simulation results as shown in Figure 5–2 that,
when the signal line is placed at the mid-height between the EBG surface and the top conductor plane, the width of the island could be as small as 0.8 mm to provide resonance-free signal transmission. And from Figure 5–4, it can be seen that the number of grounding vias can be reduced from 10 to only 2 as shown in Figure 5–3 in order to achieve optimal signal transmission. In order to accommodate the two vias of diameter of 0.2 mm and a stripline of width of 0.24 mm, the width of the island is chosen as 1 mm. The edge-to-edge distance between the strip and EBG patch are kept at 0.2 mm on each side.

Figure 5–2: $S_{21}$ of case E when the width of the island strip is 0.4, 0.6, 0.8, 1.0 and 1.2 mm.
Figure 5–3: Top view of a signal line routed above a strip island in the EBG structure with 10 grounding vias.

Figure 5–4: $S_{21}$ of case E when the number of the vias is 2 as shown in Figure 5–1 or 10 as shown in Figure 5–3.
Also, the locations of the grounding vias are varied and the impact on $S_{21}$ are observed through full-wave simulations. It is determined that the locations of the two grounding vias can be flexible. As depicted in Figure 5–1, they can be placed both in the middle of the island strip, or both at one end or the opposite ends as shown in 5–5, as long as they are symmetric with respect to the center of the signal line.

![Figure 5–5: Possibilities for placement of the grounding vias of the island strip.](image)

Adding the island strip in the EBG structure hardly increases the fabrication cost and complexity. At the same time, as it has a close configuration to that of a stripline, it should keep optimal signal integrity performance up to the highest frequency of interest, which is 10 GHz for the studied case.
5.2 Signal Integrity Evaluation

Signal integrity of the interconnect routed above the island strip of Figure 5–1 (called case E here for simplicity) is analyzed by simulation of S-parameters using Ansoft HFSS. In this studied case, the length of the signal line is 100 mm. From the $S_{21}$ result depicted in Figure 5–6, it can be observed that the signal line in case E structure exhibits a similar transmission coefficient as that of the regular stripline in Figure 3–2, which has the same strip width, length, substrate height and dielectric constant.

![Comparison of the S21 of Case E structure with that of a regular stripline from full-wave simulation.](image)

Figure 5–6: Comparison of the $S_{21}$ of Case E structure with that of a regular stripline shown in Figure 3–3 from full-wave simulation.

Another way to examine the signal integrity performance of the new structure (Case E) is by observing the return current on the EBG surface. The distribution
of the current is determined by plotting the magnitude of the current density on the EBG surface. As discussed in chapter 3, when signal line is embedded in a regular EBG-PDN, the return current couples from one EBG patch to another, and spreads over the whole EBG surface, which could cause potential EMI problems (see Figure 3–13 in Chapter 3). However, from Figure 5–7, it can be seen that the return current for Case E structure is confined on the narrow island. This is investigated at 3, 6, and 8 GHz using full-wave simulations. Thus, it is concluded that the proposed modification to the EBG-PDN structure also reduces the EMI problems.
Figure 5–7: Case E: Magnitude of the surface current density $J_{vol}$ on the EBG surface underneath the signal line at (a) 3 GHz (within the bandgap), (b) 6 GHz (outside of the bandgap), (c) 8 GHz ($f_3$).
5.3 Noise Suppression Evaluation

Adding the island strip in the EBG surface breaks its periodic pattern and can impact its stopband. Therefore, the noise suppression characteristics of the case E EBG-PDN need to be investigated by full-wave simulations. In order to verify the stopband in all azimuthal directions of propagation, several ports are placed along the x axis, y axis, and x-y diagonal directions as shown in Figure 5–8. The ports are created in the layout by using coaxial structures representing vertical mount connectors.

![Figure 5–8: The schematic of the case E structure and its ports used for simulations by Ansoft HFSS.](image)

Note that in these simulations the signal line is removed. For comparison, an EBG-PDN structure as shown in Chapter 2, Figure 2–21, is also simulated. The transmission coefficients of these two structures at different directions are plotted.
in Figure 5–9. It can be observed that the stopband along the x-axis ($S_{21}$) is reduced from 1.6 GHz (2.2 - 3.8 GHz) to 0.9 GHz (2.2 - 3.1 GHz), as expected, since port 1 and 2 are located along the strip island. Note that the island strip is not placed along the y-axis and x-y diagonal direction. The induced stopbands in these two directions almost remain the same as that of the EBG structure without the island. The stopband in $S_{43}$ and $S_{65}$ for the case without the island and with the island is 1.6 GHz (from 2.2 to 3.8 GHz). Therefore, it can be concluded that the impact of inserting the island strip on noise suppression of the EBG-PDN is minimal.

![Graph of transmission coefficients](image)

Figure 5–9: Comparison of the transmission coefficients of the EBG-PDN with and without the island strip in various azimuthal directions as shown in Figure 5–8 and 2–21, respectively.
5.4 Fabrication and Measurements

A test board based on the Case E structure containing signal line was also fabricated. The top view of the EBG surface with the island strip and signal line are shown in Figure 5–10. The board area is 80 mm by 61 mm containing 6 by 8 mushroom EBG cells with buried vias. The parameters of the EBG unit cell are the same as in the previous studied cases (\(a = 10\) mm, \(H = 0.508\) mm, \(p = 9.6\) mm, \(r = 0.2\) mm, \(g = 0.4\) mm as seen in Figure 2–16). The width of the island is 1 mm, and the width of the signal line is 0.24 mm, located in the mid-height between the top plane and the EBG surface. As shown in Figure 5–10 (b), two ring-like pads are added at (10 mm, 30.5 mm) and (70 mm, 30.5 mm) for connecting the vertical SMA connectors and feeding the transmission line. The inner diameter of the pad is 1.3 mm, the same as the diameter of the inner pin of an SMA connector pin. The width of the ring-like pad is determined as 0.5 mm for soldering convenience. The length of the signal line between the two ports is 60 mm.

Simulated and measured \(S_{21}\) plots are provided in Figure 5–11. A slight discrepancy between the simulation and the experimental results is noticed, which is due to the impedance mismatch between the 50 \(\Omega\) connectors and the ring-like pads and the vias at the ends of the signal line. Nevertheless, the measured insertion loss profile of Case E is free from strong transmission dips. As shown in Figure 5–12, the two resonance dips in the measured \(S_{21}\) of Case D prototype explained in Section 3.4.2 are not present in the measured \(S_{21}\) results for case E, which confirms the full-wave
Figure 5–10: (a) Top view of the Case E EBG surface with the island strip. (b) Top view of the signal line with the design parameters of the pads.

Time domain eye diagram measurements are also performed to compare the prototype based on Case E with those of Case D. The same eye-diagram set-up used for measurement of Case D prototype as presented in Section 3.4.3 is utilized here. The measured eye diagrams of the two prototypes are presented in Figure 5–13, and the details of measured eye diagram parameters are listed in Table 5–1 (repeated from Section 3.4.3 for convenience) and Table 5–2. It can be observed that the Case E prototype demonstrates more superior performance compared to Case D prototype, especially at higher data rates. The performance of Case D deteriorates rather
Figure 5–11: $S_{21}$ comparison for full-wave simulation results for case E and measurement results for the prototype shown in Figure 5–10.

rapidly as the data rate increases. For example when the data rate is 7 Gb/s, eye height for case D is 146.94 $mV$, while eye height for case E is 287.30 $mV$. At high data rates, a fuller spectrum exist at higher frequencies which may overlap with the dips in the $S_{21}$ of Case D structure. This in time domain presents as closing of the eyes and distortion.

Table 5–1: Parameters of fabricated prototype based on Case D.

<table>
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<th>7 Gb/s</th>
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<td>680.00</td>
<td>830.00</td>
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<tr>
<td>Eye Height (mV)</td>
<td>365.22</td>
<td>296.00</td>
<td>146.94</td>
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<tr>
<td>Eye Width (ps)</td>
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<td>Pk-Pk Jitter (ps)</td>
<td>18.00</td>
<td>33.60</td>
<td>64.50</td>
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</tbody>
</table>
Figure 5–12: $S_{21}$ comparison of measurement results for the prototype case E shown in Figure 5–10 and prototype case D presented in Section 3.4.2.

Table 5–2: Parameters of fabricated prototype based on Case E.

<table>
<thead>
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<th>data rates</th>
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<th>5 Gb/s</th>
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<td>Eye Height $(mV)$</td>
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<td>287.30</td>
</tr>
<tr>
<td>Eye Width $(ps)$</td>
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</tr>
<tr>
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<td>25.20</td>
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</tbody>
</table>
Figure 5–13: Eye diagram measurement results of Case D and Case E prototypes at the data rate of 3, 5 and 7 Gb/s.
5.5 Summary

In this chapter, a modified EBG-PDN is introduced, which contains an island strip on the regular EBG surface under the signal line to create a continuous return current path. By full-wave simulations, the design parameters of the island strip including its width and location of the grounding vias are optimized. The insertion loss results from both simulations and measurements show similar signal transmission quality as that of a conventional stripline. At the same time, the modified EBG-PDN still maintains its omni-directional stopband similar to the EBG-PDN studied in chapter 2. A test prototype based on the modified EBG-PDN is fabricated, both S-parameter and eye-diagram measurements of the fabricated prototype confirm its superior signal integrity performance compared to the EBG-PDN without the island strip.
6.1 Conclusions

This thesis provides an investigation of signal integrity issues in interconnects embedded in a PDN containing a mushroom-type PDN, i.e an EBG-PDN. It starts with an overview of the signal and power integrity problems and describes a simple power distribution network (PDN) geometry by using parallel-plate wavguide and cavity models.

The EBG structure, which is realized by 2-D periodic patterns, induces stop-bands to prevent wave propagation over a certain frequency range. Because of this frequency-selective nature, the EBG structures are incorporated in the parallel-plate PDN of modern electronic systems to suppress power/ground or simultaneous switching noise. However, the EBG takes up three of the signal routing surfaces, and therefore routing signals within the EBG-PDN become inevitable in compact and highly integrated systems.

It is shown in this thesis that signal transmission in the presence of an EBG reference plane is impaired due to the discontinuities introduced by the periodic pattern
in the return current path. A number of signal line routing scenarios in an EBG-PDN are studied using mushroom-type EBG structures with buried or through vias. When the signal line is embedded in a mushroom-type EBG-PDN, it can be routed above a row of buried vias, above the gaps between the patches or underneath them. Signal integrity evaluations using full-wave S-parameter simulations show that the transmission quality is relatively better when the signal line is routed above a row of buried vias. Nonetheless, resonance dips are observed in the $S_{21}$ profiles of all studied cases. It is found that these $S_{21}$ dips are related to the physical structure of the vias and the gaps between the patches of the mushroom-type EBG structure. In addition, the distribution of the return current path (on the EBG surface) for various routing cases is generated using full-wave solvers. It is shown that at the resonance frequencies the return current is less localized and is distributed across the substrate creating potential EMI problems.

Also, a simple lumped element model is developed to represent the EBG-PDN and extended to include all the discussed routing cases. The values of the components in the model are found from closed-form formulas and by using a quasi-static field solver. The model is portable to common SPICE-like simulators and enables fast global system simulations. It is also used to reveal the components behind the generation of the dips in the insertion loss profiles. Two LC resonance pairs are considered. The lower resonance dip is due to the inductance of the via and the parallel-plate capacitance between the patch and both of the reference planes. The higher resonance is caused by the mutual inductance and fringing capacitance
between the adjacent patches. The proposed model is validated with full-wave S-parameter simulations.

Finally, in this thesis, in order to eliminate the signal integrity problems of a signal line routed above an EBG structure, a solid conductor strip, referred to as an island, is inserted underneath the line on the EBG surface. The width of the island strip and the number of the grounding vias connecting the strip to the bottom conductor plane are optimized by full-wave simulations. The S-parameter results demonstrate that the proposed structure provides an omni-directional stopband close to what is obtained in an EBG-PDN structure without the island. When a signal line is routed above the modified EBG structure, it presents almost the same insertion loss characteristics as that of a conventional stripline. The prototype of a signal line routed above this island is fabricated. S-parameter measurements confirm the simulation results and show elimination of the resonance dips in the insertion loss profile. Also, by comparing the measured eye-diagrams of the prototype with the island to those of the fabricated prototype of a signal line routed in a mushroom-type EBG-PDN with through vias, the superior signal integrity performance of the modified EBG structure is demonstrated in the time domain.
6.2 Recommendations for Future Work

In this thesis, the signal integrity investigations only focus on single-ended lines. In practice many systems utilize differential signalling. In continuation of this research, future work may include characterization of tightly coupled differential signal lines routed in an EBG-PDN. In addition, the base model developed in this thesis for single-ended lines can also be extended to differential pairs and further system simulations can be conducted including advanced digital or analog electronic circuits.

The signal and power integrity studies presented herein only include mushroom-type EBG structure. There are other EBG geometries that have been proposed for power/ground noise suppression and they can be investigated in the same context of EBG-PDN signal integrity evaluations. Modelling of such EBG-PDNs is another challenge that can be undertaken.

In this thesis, the potential generation of EMI problems is studied by monitoring the return current distribution plots. Further in-depth investigation of these problems should be done by observing the radiation fields from the side walls of the finite EBG-PDN through simulations and measurements, especially at the identified resonance frequencies.
Appendix
Eye Diagram Measurements

The eye diagram is widely used to evaluate signal integrity characteristics of high speed systems since it provides both visual and qualitative information of the system performance. Eye diagram measurements are commonly implemented by generating a PRBS pattern which is launched into a device-under-test (DUT). The PRBS is transmitted through the DUT, and at the output a high speed sampling oscilloscope is used to monitor the output eye diagram. The eye diagram measurements in this thesis are performed using the instruments and following the procedures described below:

Equipments
1. Anritsu MP1763C pattern generator with an external trigger
2. Tektronix TDS 8200 digital sampling oscilloscope with 80E06 70 GHz sampling module (one channel)
3. Signal generator (optional, in case a tunable internal clock trigger is not available)
4. High frequency cables

Procedures
1. Connect the equipments
   A) Clock source

Option 1:
Connect the RF output (50 Ω impedance) at the rear panel of the signal generator
to the External Clock input of the pulse pattern generator with a voltage level in the range of 0.4 - 2.5 $V_{p-p}$ as shown in Figure 6–1 [59].

![Figure 6–1: Eye diagram measurement set-up.]

**Option 2:**

Use the built-in synthesized clock generator on the pulse pattern generator panel as shown in Figure 6–2 [60].

B) Use adapter between the cables and channel connectors. The $DATA$ or ($DATA$) output of the pattern generator connects to the input channel of the oscilloscope. The $CLOCK$ or ($CLOCK$) connects to the trigger connector of the oscilloscope.

2. Set up the measurement conditions

A) Switch on the power of the generators first, then switch on the power to the
oscilloscope. Do not press any instrument keys until the program is loaded [61].

Pulse Pattern Generator:

B) Set the built-in clock generator to the desired data rate (e.g. a 1 GHz clock will generate a train of RBPS pattern at data rate of 1 Gb/s).

C) Choose the desired PRBS pattern using the seven options ($2^7 - 1$ to $2^{31} - 1$), six frames of STM-64/STS192, or with randomness and mark ratio variance [60].

D) Five output ports:
Independent values can be set for the offset and output amplitude of both $DATA$ and $(DATA)$. When independency is not required, the clock outputs can be used since they are complimentary $CLOCK$ and $(CLOCK)$.
$CLOCK2$ output is with a fixed offset and amplitude [60].
High Speed Oscilloscope:

E) Start the 80SJNB application

F) Start → All Programs → Tektronix Applications → 80SJNB → 80SJNB

1) Select source: CH1

2) Press the SETUP DIALOGS button on the instrument

Select Trigger Source:

3) In the Setups dialog box, select the Trig tab. Select External Direct as the trigger source with signal up to 3.0 GHz. Select External Prescale as the trigger source with signal from 2.0 GHz to 12.5 GHz. If the channel is connected to the Pattern Sync connector of the pattern generator as shown in Figure 6–2, set the trigger source to Pattern Sync [62].

4) Enter the Data Rate and Pattern Length.

3. Setup the 80SJNB Application

A) Press the Acquisition MENU button to display the acquisition setup dialog box.

B) Select the acquisition dialog box. In order to show PRBS output data select the acquisition mode to average. In order to display the eye pattern, select the acquisition mode to sample, select condition from Stop After list, and enter the number of acquisition [62].

C) Start acquisition, and wait till the message analysis complete is displayed. Once the cycle is complete, the results are displayed. Adjust horizontal and vertical
scale to show the desired waveform.

D) Select File → Save Settings to open the Save dialog box, select the directory to save the setup file. The application appends a "STP" extension to the name of the file. Next time, select file → Recall Settings to recall the setup [63].

4. Display the results
   
   A) View → 1-up, 2-up or 4-up to show the plot windows to fill the entire screen.

   B) For each plot window, select a type of plot to display. Right-click anywhere on the existing plot display to select a plot from the plot categories (Jitter, Noise, Eyes, Patterns or SSC).

   For eye diagram measurements, it usually uses PDF Eyes under Eye plots function. Then adjust SO In, SP Filter, SP channel and SP Equalizer to capture the proper eye pattern [63].

   C) Use the tool bar to select how the numerical results are displayed, for example, Eye Opening and Eye Amplitude.
References


[59] Anritsu. MP1763C/MP1764C/MP1764D Pulse Pattern Generator/Error Detector Data Sheet.

[60] Anritsu. MP1763C/MP1764C Technical Note.
